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New editions of this manual will incorporate all material updated since the previous edition. The manual printing date, which indicates the manual’s current edition, changes when a new edition is printed. Minor corrections and updates which are incorporated at reprint do not cause the date to change. Update packages may be issued between editions and contain additional and/or replacement pages to be merged into the manual by the user. Note that pages which are rearranged due to changes on a previous page are not considered to be revised.

Edition: REV1.0
Date: 22 June 2006
Software Version: 3.1
Getting Help

If you have any questions while you are using Ansoft SIwave you can find answers in several ways:

- **Ansoft SIWave Online Help** provides assistance while you are working.
  - To get help about a specific, active dialog box, click the Help button in the dialog box or press the **F1** key.
  - Select the menu item **Help > Contents** to access the online help system.
- **Tool tips** are available to provide information about tools on the toolbars or dialog boxes. When you hold the pointer over a tool for a brief time, a tooltip appears to display the name of the tool.
- As you move the pointer over a tool or click a menu item, the **Status Bar** at the bottom of the product window provides a brief description of the function of the tool or menu item.
- The Ansoft SIwave Getting Started guide provides detailed information about using SIwave to create and solve signal integrity projects.

- **Ansoft Technical Support**
  - To contact Ansoft technical support staff in your geographical area, please log on to the Ansoft corporate website, [www.ansoft.com](http://www.ansoft.com) and select **Contact**.
  - Your Ansoft sales engineer may also be contacted in order to obtain this information.

**Visiting the Ansoft Web Site**

If your computer is connected to the Internet, you can visit the Ansoft Web site to learn more about the Ansoft company and products.

- From the Ansoft Desktop
  - Select the menu item **Help > Ansoft Corporate Website** to access the Online Technical Support (OTS) system.
- From your Internet browser
  - Visit [www.ansoft.com](http://www.ansoft.com)
Getting Help

For Technical Support

The following link will direct you to the Ansoft Support Page. The Ansoft Support Pages provide additional documentation, training, and application notes.

- Web Site: http://www.ansoft.com/support.cfm
- Technical Support:
  - 9-4 EST:
    - Pittsburgh, PA
      - (412) 261-3200 x0 - Ask for Technical Support
    - Burlington, MA
      - (781) 229-8900 x0 - Ask for Technical Support
  - 9-4 PST:
    - San Jose, CA
      - (408) 261-9095 x0 - Ask for Technical Support
    - Portland, OR
      - (503) 906-7944 or (503) 906-7947
    - El Segundo, CA
      - (310) 426-2287 - Ask for Technical Support
WebUpdate

This new feature allows you to update any existing Ansoft software from the WebUpdate window. This feature automatically scans your system to find any Ansoft software, and then allows you to download any updates if they are available.
Board Design

The board design example is intended to show you how to import, simulate, and analyze a 4-layer board structure using SIwave.

When traces are routed through power and ground planes, you can experience signal integrity problems. The following illustration details the board design that will be used in SIwave to investigate the following SI applications:

- How resonant behavior effects signal transmission along a trace
- Non-ideal plane behavior

For this example, we will import the design file and its discrete components. After defining the correct capacitance, ESL, and ESR values, a resonant mode calculation will be performed. We will then add decoupling capacitors to the planes to see if an improvement can be made in the resonant mode voltage swing.
Ansoft SIwave Design Environment

The following features of the Ansoft SIwave Design Environment are used to create this passive device model:

- **Importing**
  - ANF file
  - Component File
- **Editing Component Values**
  - Capacitance
  - ESL
  - ESR
- **Boundary/Sources**
  - Ports
- **Solutions**
  - Resonant Modes
  - S-Parameters
  - Full Wave Spice Sub-circuit
- **Fields**
  - Resonant Mode Plot
- **Plots**
  - S-Parameter sweep
Creating a New SIwave Project

To launch SIWave program, click the Microsoft Start Button, select Programs, select Ansoft, then select the SIwave 3.0 program group. Select the executable SIwave 3.0.

Import the .ANF

To import the .anf file
1. Click File > Import > ANF
2. Navigate to the file named siwave_board.anf
3. Click OPEN

Import the .CMP

To import the .cmp file
1. Click File > Import > Component File
2. Navigate to the file named siwave_board.cmp
3. Click OPEN

Save the .siw file

To save the .siw file
1. Click File > Save As
2. Filename: siwave_board.siw
3. Click OK
Changing the View

**Toolbar**

- Pan
- Zoom in
- Fit All
- Rotate
- Dynamic Zoom
- Zoom Out
- Top-down View

**Shortcuts**

Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:

- **ALT + Drag** - Rotate
- **ALT + Shift + Drag** - Dynamic Zoom

In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.

- **Shift + Drag** - Pan

**Predefined View Angles**

- Top
- Left
- Right
- Bottom
## Setting Simulation Global Options

In the SIwave toolbar, click *Simulation -> Options*

- Under the **Plane Void Meshing**, place mark in radial button for
  *Automatically determine which voids to mesh*
- Under **Trace Coupling**, place check mark next to
  *Only consider signal traces during coupling analysis*
- Under **Mesh Refinement**, click radial button for
  *Automatic*
- Under **Boundary Condition To Use**, click radial button for
  *Open Boundary*

Place check mark next to:

- Ignore nets named "DUMMY" or "Unused" during simulation
- Perform ERC during simulation setup

Click OK to exit.
Example - Board Design

Verify the Layer Stackup

To view the board layers:

1. Click **Edit -> Layer Stackup**. Or use the hotkey.
2. Click **OK** when done.
**Editing the Capacitance Values**

To define the correct capacitance, ESL, and ESR values for every capacitor group that was imported:

1. Click the **Circuit Elements** tab
2. Expand **Capacitors** by clicking the plus sign next to it
3. Expand **Local** by clicking the plus sign next to it
4. Highlight **CAPACITOR_CDR02**
5. Right click **CAPACITOR_CDR02** and select **Edit Component Properties**
   1. Capacitance: **1E-007**
   2. Parasitic Inductance: **1E-009**
   3. Parasitic Resistance: **0.05**
6. Click **OK**
Example - Board Design

⚠️ Editing the Capacitance Values (con’t)

⚠️ To define the correct capacitance, ESL, and ESR values for the remaining Capacitor groups

1. Highlight **CAPACITOR_CDR04**
2. Right click **CAPACITOR_CDR04** and select **Edit Component Properties**
   1. Capacitance: **1E-007**
   2. Parasitic Inductance: **1E-009**
   3. Parasitic Resistance: **0.05**
   4. Click **OK**

3. Highlight **CAPACITOR_CDR06**
4. Right click **CAPACITOR_CDR06** and select **Edit Component Properties**
   1. Capacitance: **1E-007**
   2. Parasitic Inductance: **1E-009**
   3. Parasitic Resistance: **0.05**
   4. Click **OK**

5. Highlight **CAPACITOR_CSR13B**
6. Right click **CAPACITOR_CSR13B** and select **Edit Component Properties**
   1. Capacitance: **1E-007**
   2. Parasitic Inductance: **1E-009**
   3. Parasitic Resistance: **0.05**
   4. Click **OK**

7. Highlight **CAPACITOR_CWR06-10V,47,10%**
8. Right click **CAPACITOR_CWR06-10V,47,10%** and select **Edit Component Properties**
   1. Capacitance: **4.7E-005**
   2. Parasitic Inductance: **1E-008**
   3. Parasitic Resistance: **0.5**
Running a Resonant Mode Simulation

To run an eigenmode simulation

1. Click Simulation -> Compute Resonant Modes
2. Minimum Frequency: 2.55238E+008
3. Maximum Frequency: 2e9
4. # of Modes to Compute: 5
5. Click OK

When the Resonant Mode Results screen comes up, the solution is done,

1. To view the Voltage plots for the 5 resonant modes, you have to select the 2 planes to plot the voltage in between.
2. Under Plot voltage difference between planes on,
   1. Change the first pull down to L2
   2. Change the second pull down to L7
   3. Click Compute
3. When the computation is done, you can view the various voltage plots for each mode by highlighting the modes in the bottom section of the Resonant Mode Results window.
Example - Board Design

**Phase Animation**

To view the phase animation for a resonant mode:

1. In the **Resonant Mode Results** window, in the bottom section, highlight the 4\(^{th}\) resonant mode (0.656 GHz) with Plot Layer L2 and Reference Layer L7
2. Click **Phase Animation**
3. In the Phase Animation window, Click **Generate Frames**
4. When all 18 frames are generated, Click the **play button**
5. When done viewing the animation, click **Close**
6. Click **Close** to close the **Resonant Mode Results** window

Note: To turn off the mesh display, click **View -> Mesh**

Note: To turn off the Display Color Scale, click **View -> Voltage Color Display**
Adding Capacitors to the model

At the 4th resonance, we see that there is a large voltage swing in the top right hand corner of the board file. We will add capacitors in that area to try and reduce the effects of the resonance in that area.

Return to the top down view for editing.

To add capacitors:

1. Turn off the Voltage Surface plot, if not already done, by clicking View > Voltage Surface Plot.
2. Click Circuit Elements -> Capacitor.

Place a capacitor from part list CAPACITOR_CDR02:

1. For the Positive Node enter coordinates x: 8200 y: 5400.
2. For the Negative Node enter coordinates x: 8400 y: 5400.
3. At the Select Layers for capacitor terminals screen
   1. Highlight L2 for the Positive Terminal.
   2. Highlight L7 for the Negative Terminal.
   3. Click OK.
4. At the Set Capacitor Parameters screen
   1. Reference Designator: C65.
   2. Part Number: CAPACITOR_CDR02.
   3. Click OK.

Place a capacitor that is not from a parts list:

1. For the Positive Node enter coordinates x: 8200 y: 5300.
2. For the Negative Node enter coordinates x: 8400 y: 5300.
3. At the Select Layers for capacitor terminals screen
   1. Highlight L2 for the Positive Terminal.
   2. Highlight L7 for the Negative Terminal.
   3. Click OK.
4. At the Set Capacitor Parameters screen
   1. Reference Designator: C66.
   2. For Part Number, type: new_cap.
   5. Parasitic Resistance: 0.05.
   6. Click OK.
Re-run the Resonant Mode Simulation

To re-run an eigenmode simulation

1. Click **Simulation -> Compute Resonant Modes**
2. Minimum Frequency: **2.55238E+008**
3. Maximum Frequency: **2E+009**
4. # of Modes to Compute: **5**
5. Click OK

When the Resonant Mode Results screen comes up, the solution is done,

To view the Voltage plots for the 5 resonate modes, you have to select the 2 planes to plot the voltage in between.

1. Under **Plot voltage difference between planes on**,
   1. Change the first pull down to L2
   2. Change the second pull down to L7
   3. Click **Compute**

2. View the 4th resonant mode plot again. You will now see that the voltage swing in the top right hand corner of the board where the capacitors were placed is now showing very little swing.
Frequency Sweep to Verify Resonances

In the first part of this chapter, we imported in a design file with discrete components on it. We ran a resonant mode simulation and viewed the results. For one of the resonances, we added 2 decoupling capacitors to decrease the resonant mode voltage swing in that area, and we saw that the capacitors worked.

We will now place a port on a specific point on the power/ground planes to see if the frequency sweep can pick up the same resonances that the eigenmode solver is reporting.

Rerunning the Resonant Mode Simulation

Click *Simulation -> Compute Resonant Modes*

1. Don’t change the **Minimum Frequency** value.
2. Maximum Frequency: **2E+009**
3. # of Modes to Compute: **10**
4. Click **OK**

When the Resonant Mode Results screen comes up, the solution is done,

1. To view the Voltage plots for the 10 resonate modes, you have to select the 2 planes to plot the voltage in between.
2. Under **Plot voltage difference between planes on**,
   1. Change the first pull down to L2
   2. Change the second pull down to L7
   3. Click **Compute**
3. When the computation is done, you can view the various voltage plots for each mode by highlighting the modes in the bottom section of the Resonant Mode Results window.
Example - Board Design

Placing a Port
- When scrolling through the various 10 resonant mode plots, you will notice that in the bottom right hand corner of the board seems to have a lot of activity in several modes. Modes 2, 3, 6, 7, and 8 in particular have a lot of activity in the bottom right hand corner.

Mode 2

Place port
- Return to the top down view to editing
  - Click **Close** to close the Resonant Mode Results window
  - Click **View -> Top-Down View**
- To add capacitors:
  1. Turn off the **Voltage Surface plot**, if not already done, by clicking **View -> Voltage Surface Plot**
  2. Click **Circuit Elements -> Port**
- Place a port
  1. For the **Positive Node** enter coordinates $x: 8500$  
     $y: -150$ then click Enter
  2. For the **Negative Node** enter coordinates $x: 8650$  
     $y: -150$ then click Enter
**Example – Board Design**

⚠️ **Place ports con’t**

1. For the Positive Terminal, select **L2: GND**
2. For the Negative Terminal, select **L7: VCC**, then click **OK**
3. In the Port Properties window, change the name of the port to **p1**, then click **OK**

**Select layers for port terminals**

**Port Properties**

- **Name:** p1
- **Reference Impedance:** 50 Ohms

- Positive Terminal Net: GND
- Negative Terminal Net: VCC
- Positive Terminal not connected to Pin or Pingroup
- Reference Terminal not connected to Pin or Pingroup
### Computing S-parameter

- **Click** *Simulation -> Compute S, Y, Z Parameters*
  1. Start Frequency: **200E+006**
  2. Stop Frequency: **1.5E+009**
  3. Number of Solution Points: **300**
  4. Sweep Selection: **Interpolating Sweep**
  5. **Click OK**

- **When the Ansoft SIwave Reporter opens up:**
  - The S-parameter frequency sweep for **p1** should be displayed, if not:
    - **In the Project tree for siwave_board, under Results, double click S-Parameter**
    - Notice the resonance dips in the s-parameter plots. They correspond to the resonances from the eigenmode solve

#### Eigenmode Resonant Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>f(GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.549340226</td>
</tr>
<tr>
<td>3</td>
<td>0.640807129</td>
</tr>
<tr>
<td>6</td>
<td>0.769669019</td>
</tr>
<tr>
<td>7</td>
<td>0.867564282</td>
</tr>
<tr>
<td>8</td>
<td>0.946752343</td>
</tr>
</tbody>
</table>

![Graph of S-parameter frequency sweep](image)
**Frequency Sweep to Verify Resonances**

In the first part of this chapter, we imported in a design file with discrete components on it. We ran a resonant mode simulation and viewed the results. For one of the resonances, we added 2 decoupling capacitors to decrease the resonant mode voltage swing in that area, and we saw that the capacitors worked.

We are now going to show the effects of having a driven signal in the vicinity of a resonance. We will be placing a Voltage source on a net and then seeing the frequency response of that signal as it passes through the resonance area. This will show how strong the coupling can be when signal nets are near resonances.

**Rerunning the Resonant Mode Simulation**

1. Click **Simulation -> Compute Resonant Modes**
2. Don’t change the **Minimum Frequency** value
3. Maximum Frequency: **2E+009**
4. # of Modes to Compute: **10**
5. Click **OK**

When the Resonant Mode Results screen comes up, the solution is done,

1. To view the Voltage plots for the 10 resonate modes, you have to select the 2 planes to plot the voltage in between.
2. Under **Plot voltage difference between planes on**,
   1. Change the first pull down to **L2**
   2. Change the second pull down to **L7**
   3. Click **Compute**
3. When the computation is done, you can view the various voltage plots for each mode by highlighting the modes in the bottom section of the Resonant Mode Results window.
Viewing Resonances Near Signal Nets

When scrolling through the various resonant mode plots, you will notice that in Mode 9, there is quite a bit of voltage swing in a few places on the board. We are going to focus in a net named P_TLM_ERR that seems to cross into this resonance.

Place Voltage Source

Return to the top down view for editing

Click Close to close the Resonant Mode Results window

Click View -> Top-Down View

To add voltage source:

1. Turn off the Voltage Surface plot, if not already done, by clicking View -> Voltage Surface Plot
2. Click Nets tab
3. Select P_TLM_ERR from net list
4. Click Circuit Elements -> Voltage Source

Place a voltage source

1. For the Positive Node enter coordinates \( x: 1150 \quad y: 3775 \) then click Enter
2. For the Negative Node enter coordinates \( x: 1150 \quad y: 3775 \) then click Enter
Place Voltage Source con’t

1. For the Positive Terminal, select Surface: P_TLM_ERR
2. For the Negative Terminal, select L2: GND, then click OK
3. Set Voltage Source Properties
   1. Magnitude: 0.5 Volts
   2. Parasitic Resistance: 0.01 Ohms
Example - Board Design

Place Voltage Probe
- To add voltage probe:
  - Click Circuit Elements -> Voltage Probe
- Place a voltage probe
  1. For the **Positive Node** enter coordinates \( x: 4325 \)
     \( y: 2235 \) then click Enter
  2. For the **Negative Node** enter coordinates \( x: 4325 \)
     \( y: 2235 \) then click Enter
  3. For the Positive Terminal, select **Surface: P_TLM_ERR**
  4. For the Negative Terminal, select **L2: GND**, then click **OK**
  5. Edit Probe Name: **VPROBE1**
  6. Click **OK**

Frequency Sweep Setup
- Click **Simulation** \( \rightarrow \) **Compute Frequency Sweep**
  1. Start Frequency: **1E+8**
  2. Stop Frequency: **1.75E+9**
  3. Plot magnitude at all probes:: ☑ **Checked**
  4. Click **OK**

Viewing results
- The Mag(VPROBE) plot should be displayed after the solution is complete
Correlating Peak Voltages with Frequency Sweep Plots

When looking at the Voltage vs. Frequency plots, you will see that there are voltage spikes at 267MHz, 850MHz, and 1.48GHz. This means that at around these frequencies, there is a resonant mode that is coupling onto the trace and increasing the voltage already on the signal. You can see a visual of these resonant frequency points by viewing the Surface Voltages.

Viewing the Surface Voltages

1. Minimize the Ansoft SIwave Reporter window
2. The Frequency Sweep Results window should be visible. If not click Results → Frequency Sweep → Surface Voltages
3. Turn on the Surface Plots by clicking View → Voltage Surface Plot
4. Click the Play button

267MHz

850MHz

1.5GHz
Example - Board Design

- **Effect of ESL and ESR**
  - In this chapter we will look at the effect of Effective Series Inductance and Effective Series Resistance on an impedance simulation. ESL and ESR are values that can be entered into capacitor properties. These values have a profound effect on frequency and amplitude of resonant modes. This example will show the effects of changing these values.
  - We will use the same model from Chapter 1b for this example.

- **Plotting Impedance**
  - As mentioned before, we will be using results from the previous example. If the Ansoft SIwave Reporter is not already displayed, then bring up it up by doing the following:
    1. Select Results -> S, Y, Z Parameters -> Plot Magnitude/Phase
    2. In the project window expand the project named `siwave_board`
    3. Expand the model named `siwave_board`
    4. Expand Results
    5. Double click Z-Parameters to bring up the Impedance sweep plot
    6. Right click on the plot and choose Accumulate
    7. Minimize this screen and return to the SIwave screen

- **Changing ESL values**
  - To globally change the ESL values for 4 capacitor part names:
    1. Select the **Circuit Elements** tab
    2. Expand Capacitors
    3. Expand Local
    4. Highlight CAPACITOR_CDR02
      1. Right click CAPACITOR_CDR02
      2. Select Edit Component Properties
      3. Change Parasitic Inductance to 2E-009
      4. Click OK
Example – Board Design

5. Highlight CAPACITOR_CDR04
   1. Right click CAPACITOR_CDR04
   2. Select Edit Component Properties
   3. Change Parasitic Inductance to 2E-009
   4. Click OK

5. Repeat this procedure for CAPACITOR_CDR06, and CAPACITOR_CSR13B

△ Re-run the S-Parameter sweep
   1. Click Simulation -> Compute S, Y, Z Parameters
   2. Start Frequency: 2E+008
   3. Stop Frequency: 1.5E+009
   4. Number of Solution Points: 300
   5. Sweep Selection: Interpolating Sweep
   6. Click OK
Viewing the overlaid results

To view the results of the new s-parameter sweep

1. Maximize the Ansoft SIwave Reporter window

You will now see the 2 plots overlaid on each other. You can see that changing ESL values shifts the resonance frequencies.
Changing ESR values

To globally change the ESR values for 4 capacitor part names:

1. Minimize this screen and return to the SIwave screen
2. Select the Circuit Elements tab
3. Expand Capacitors
4. Expand Local
5. Highlight CAPACITOR_CDR02
   1. Right click CAPACITOR_CDR02
   2. Select Edit Capacitor Properties
   3. Change Parasitic Resistance to 0.5
   4. Click OK
5. Highlight CAPACITOR_CDR04
   1. Right click CAPACITOR_CDR04
   2. Select Edit Capacitor Properties
   3. Change Parasitic Resistance to 0.5
   4. Click OK
6. Repeat this procedure for CAPACITOR_CDR06, and CAPACITOR_CSR13B
**Example – Board Design**

▲ **Re-run the S-Parameter sweep**
  1. Click *Simulation -> Compute S, Y, Z Parameters*
  2. Start Frequency: 2E+008
  3. Stop Frequency: 1.5E+009
  4. Number of Solution Points: 300
  5. Sweep Selection: *Interpolating Sweep*
  6. Click OK

▲ **Viewing the overlaid results**
  1. To view the results of the new s-parameter sweep
    1. Maximize the Ansoft Siwave Reporter window
  2. You will now see the 3 plots overlaid on each other. You can see that changing ESR values shifts the amplitude of resonances.

![Graph showing the effect of changing ESR value to 0.5 on resonances]
**Example - Board Design**

- **Save SIwave Project**
  - To save SIwave project:
    1. Select *File -> Save As*
    2. File name: *board_design*
    3. Click *Save*

- **Exit SIwave**
  - Select *File -> Exit*
**Example - Package Planes Impedance**

**Package Planes Impedance Profile**

The example is intended to show you how to simulate Z-parameters on a 4 layer package structure using SIwave.

You will learn how to:
1. Import ANF and CMP files
2. Edit layer stack up
3. Create solder balls
4. Create bond wires
5. Group VCC and GND pins on both the die and ball sides
6. Generate ports
7. Compute Z-parameters analysis
8. Move around SIwave Reporter
Ansoft SIwave Design Environment

The following features of the Ansoft SIwave Design Environment are used to create this passive device model

Import
- Ansoft Neutral File (ANF)
- Components file (CMP)

Physical Geometry
- Layer stack up
- Bond wires
- Solder balls

Pre-processing
- Group pins
- Automatic ports generation

Boundary/Sources
- Ports

Solutions
- Z-Parameters

Plots
- Z-Parameter sweep
Creating a New SIwave Project

- Click the Microsoft **Start** Button, select *All Programs -> Ansoft -> SIwave 3* -> *Slwave 3* program.
- This will bring up SIwave3 window with empty project
- Click **File -> Import -> ANF**, browse to the folder that contains `siwave_bga.anf`, select `siwave_bga.anf`, and click *Open*.
- Click **File -> Import -> Component File**, browse to the folder that contains `siwave_bga.cmp`, select `siwave_bga.cmp`, and click *Open*. 
### Validation Check

It is a good idea to do a validation check before you start working on any design that you just imported into SIwave.

The **Validation Check** consists of self-intersecting polygons, disjoint nets, overlapping nets (dc-shorted) and nets with overlapping vias checks.

The last thing you want to find out is that you need a new layout after all the settings and ports have been defined.

To do a validation check:

1. Select **Edit -> Validation Check**
2. Click **Start** button to start the validation
3. When the validation is completed, you should see a window like below

4. There is no layout and DRC related problems with this design. Net names will be listed in the message window if there are any problems.
5. Click **Close** to exit the Validation Check window.
Setting Simulation Global Options

In the SIwave menu bar, click **Simulation -> Options**

1. Under **Plane Void Meshing**, click radial button for **Automatically determine which voids to mesh**
2. Under **Trace Coupling**
   - Trace Coupling Distance: **10 mils**
   - Min Coupled Trace Length: **10 mils**
   - Only consider signal traces during coupling analysis: ☑ Checked
3. Under **Solver**, set the number of CPUs if you have SIwave multi processor license
4. Under **Mesh Refinement**, click radial button for **Automatic**
5. Under **Boundary Condition to Use**, click radial button for **Open Boundary**
6. Ignore nets named “DUMMY” or “Unused” during Simulation: ☑ Checked
7. Perform ERC during simulation setup: ☑ Checked
8. Click OK to exit
Set Model Units

To set the units:

1. At the bottom right corner of the window, change the unit to **mils**

Edit Layer Stackup

To edit layers:

1. Click **Edit -> Layer Stack**. Or use the Toolbar hotkey

2. Hold down the **CTRL** key, select **UNNAMED_1** and **UNNAMED_10** layers
3. Click **Delete Selected Layers**
4. Click **OK** to confirm deletion.

   SIwave solver doesn’t allow zero thickness layer other than the bond wire layer.

5. Click **OK** to exit Layer Stack-up Editor window.
Assign Bond Wires Profile

To assign bond wires profile:

1. Click *Edit -> Bondwire Model*, or click on Toolbar button
2. Select **JEDEC 4-Point** from the **Model** listing
3. Radius: 0.5 mils
4. h1: 8 mils
5. h2: 2 mils
6. To see how is h1 and h2 measured
   Static Diagram: ☑ Checked

7. Click OK to exit

If you have multiple loop heights for the bond wires, you will have multiple names listed under **Layer**. You will then assign different profile to each **Layer** name.
Changing the View

Toolbar

Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:

- **ALT + Drag** - Rotate
- **Shift + Drag** - Pan
- **ALT + Shift + Drag** - Dynamic Zoom

In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.

Predefined View Angles

Top

Left

Right

Bottom
View Bond Wires in 3D with the Layout

- You can rotate and zoom into the die area to view the bond wires.

- To view bond wires with actual dimension, instead of a wire with zero thickness:
  - Fill the SURFACE layer display.
Assign Solder Balls Dimension

To assign solder balls dimension:

1. Click **Edit -> Solderballs**
2. Generate Solderballs: ✔ Checked
3. Add balls to padstack: BGAPAD
4. Radius: 11.5 mils
5. Height: 25 mils

6. Click OK to exit

**SIwave PCB** layer is added to the stackup after the solder balls are added to BGAPAD padstack. This layer tells SIwave where the solder balls end (solderballs start at BASE layer)
View Solder Balls

- You can rotate and zoom to see the solder balls.

Edit Material Surrounding Solder Balls

- To edit the material surrounds solder balls:
  1. Click *Edit -> Layer Stack*.
  2. Select *Bottom Dielectric* layer.
  3. Click *Edit Layer Properties*.
  4. Material: *Air*.
  5. Click OK to exit *Layer Properties* window.
  6. Click OK to exit *Layer Stack-up Editor* window.

Layer Stack-up Editor

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Film</th>
<th>Material</th>
<th>Thickness (mils)</th>
<th>Elevation (mils)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SURFACE</td>
<td>WIRESBOND</td>
<td></td>
<td>gold</td>
<td>0</td>
<td>41.75</td>
</tr>
<tr>
<td>TOP_COND</td>
<td>METAL</td>
<td>POSITIVE</td>
<td>copper</td>
<td>1.44</td>
<td>40.32</td>
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<td>UNNAMED_4</td>
<td>DIELECTRIC</td>
<td></td>
<td>FR4_epoxy</td>
<td>3</td>
<td>37.32</td>
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<tr>
<td>VCC</td>
<td>METAL</td>
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<td>35.88</td>
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<td></td>
<td>FR4_epoxy</td>
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<td>30.80</td>
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<td>POSITIVE</td>
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<td>1.44</td>
<td>25</td>
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<td></td>
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<td>0.688976</td>
</tr>
<tr>
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<td>METAL</td>
<td>NEGATIVE</td>
<td>copper</td>
<td>0.688976</td>
<td>0</td>
</tr>
</tbody>
</table>
Grouping VCC and GND Pins

To group all GND and VCC balls:

1. Click **Edit -> Create Pin Groups**
2. Part Name: **BGA**
   - This means we will be grouping pins on a part called **BGA**, it is the solder balls in this case.
3. Refdes: **P1**
   - For PCB and stacked die application, you will have multiple instances of the same part, make sure you select the right reference designator here.
4. Under Nets,
   - GND: ☑ Checked
   - Select all pin names under **GND** net. You should see all the pins in the display window are now highlighted in yellow.
5. Click **Create Pin Group**
6. Click **OK** to accept the default **P1_GND_Group** name, where **P1** is the reference designator for **BGA** part.
7. Under Nets,
   - GND: ☐ Unchecked
   - VCC: ☑ Checked
   - Select all pin names under **VCC** net. You should see all the pins in the display window are now highlighted in yellow.
8. Click **Create Pin Group**
9. Click **OK** to accept the default **P1_VCC_Group** name, where **P1** is the reference designator for **BGA** part.

You should have 2 pin groups, **P1_GND_Group** and **P1_VCC_Group** listed at the top right hand corner of the Pin Grouping Dialog window.
To group all GND and VCC wires:

1. Part name: DIE
   - This means we will be grouping pins on a part called DIE, it is the bond wires in this case.
2. Refdes: D1
3. Under Nets,
   - GND: ☑ Checked
   - Select all pin names under GND net. You should see all the pins in the display window are now highlighted in yellow.
4. Click Create Pin Group
5. Click OK to accept the default D1_GND_Group name, where D1 is the reference designator for DIE part.
6. Under Nets,
   - GND: ☐ Unchecked
   - VCC: ☑ Checked
   - Select all pin names under VCC net. You should see all the pins in the display window are now highlighted in yellow.
7. Click Create Pin Group
8. Click OK to accept the default D1_VCC_Group name, where D1 is the reference designator for DIE part.
   - You should have 2 pin groups, D1_GND_Group and D1_VCC_Group listed at the top right hand corner of the Pin Grouping Dialog window.
9. Click OK to exit Pin Grouping Dialog window
Create Port between VCC and GND on the BGA Side

To create port between VCC and GND groups on the BGA side:

1. Click **Edit -> Generate Circuit Elements**
2. Part name: **BGA**
3. Reference Designator: **P1**
4. Scroll down the scroll bar for **Circuit Element Positive Terminal** to the end, expand **Pin Groups**, select **P1_VCC_Group**
5. Scroll down the scroll bar for **Circuit Element Negative Terminal** to the end, expand **Pin Groups**, select **P1_GND_Group**
6. Circuit Element Type: **Port**
7. Click on **Create**
8. Name: **p1**
9. Click **OK**

Port **p1** has just been created between **P1_VCC_Group** and **P1_GND_Group**.

Expand **Ports** under **Circuit Elements** column, you will see port **p1** is listed there.
Create Port between VCC and GND on the DIE Side

To create port between VCC and GND groups on the DIE side:
1. Part name: DIE
2. Reference Designator: D1
3. Scroll down the scroll bar for Circuit Element Positive Terminal to the end, expand Pin Groups, select D1_VCC_Group
4. Scroll down the scroll bar for Circuit Element Negative Terminal to the end, expand Pin Groups, select D1_GND_Group
5. Circuit Element Type: Port
6. Click on Create
7. Name: p2
8. Click OK

Port p2 has just been created between D1_VCC_Group and D1_GND_Group

Expand Ports under Circuit Elements column, you will see ports p1 and p2 are listed there

9. Click OK to exit Circuit Element Generation Dialog window
**Verify Ports**

To Verify the ports we just created exist and we didn’t make mistake in terminal connections

1. Click *Edit -> Circuit Element Parameters*
2. Click on *Ports* tab
3. Verify that ports *p1* and *p2* have the right reference impedance, port positive and negative nets and terminals
4. Click *OK* to exit *Circuit Element Properties* window
Computing Z-Parameters

To compute the z-parameters:

1. Click Simulation -> Compute S-, Y-, Z-Parameters
   - Change the settings to as shown below

   ![](image)

   - Click OK to start the simulation

2. When the simulation is completed, SIwave Reporter will be launched automatically with the impedance plots loaded.

   ![](image)
Moving Around SIwave Reporter

To change the plot to log-log scale:
1. Click on the Freq text on the X-axis to highlight it
2. Double click to bring up X Axis Properties window
3. Click on Scaling tab, change the settings to as show below
4. Click OK to exit.
5. Click on any texts on the Y-axis to highlight the texts
6. Double click to bring up Y Axis Properties window
7. Click on Scaling tab, change the settings to as show below
8. Click OK to exit.
When done viewing the Z-Parameters, select File -> Exit
Click Yes to save the changes

Save SIwave Project
To save SIwave project:
1. Select File -> Save As
2. File name: bga_z-para
3. Click Save

Exit SIwave
Select File -> Exit
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Example - Package S-parameters

Package S-parameters

The example is intended to show you how to simulate S-parameters on a 4 layer package structure using SIwave.

You will learn how to:

1. Create ports using automatic port generation feature
2. Compute S-parameters
3. Simulate crosstalk with Touchstone file in Ansoft Designer
4. Compute differential S-parameters
5. Export Full Wave Spice (frequency dependent) subcircuit
6. Export RLGC subcircuit
Example - Package S-parameters

- **Ansoft SIwave Design Environment**
  - The following features of the Ansoft SIwave Design Environment are used to create this passive device model
    - **Pre-processing**
      - Automatic ports generation
    - **Boundaries/Sources**
      - Ports
    - **Solutions**
      - S-Parameters
      - Differential S-parameter
      - Crosstalk (transient) simulation with Ansoft Designer
    - **Plots**
      - S-Parameter sweep
      - Differential S-Parameter sweep
    - **Export**
      - Full Wave Spice subcircuit
      - RLG C matrices and subcircuit
Open a Slwave Project

- Click the Microsoft Start Button, select All Programs -> Ansoft -> Slwave 3
- This will bring up Slwave3 window with empty project
- Click File -> Open, browse to the folder that contains siwave_ch4_bga_s-para.siw, select siwave_ch4_bga_s-para.siw, and click Open.
- This project has the correct dimensions and materials for layer stack up, bond wires and solder balls. Please see Chapter 3 if you need to learn how to set up the above items in Slwave.
Validation Check

It is a good idea to do a validation check before you start working on any design in SIwave for the first time.

The Validation Check consists of self-intersecting polygons, disjoint nets, overlapping nets (dc-shorted) and nets with overlapping vias checks.

The last thing you want to find out is that you need a new layout after all the settings and ports have been defined.

To do a validation check:
1. Select *Edit -> Validation Check*
2. Click *Start* button to start the validation
3. When the validation is completed, you should see a window like below

4. There is no layout and DRC related problem with this design. Net names will be listed in the message window if there are any problems.
5. Click *Close* to exit the Validation Check window.
Setting Simulation Global Options

In the SIwave menu bar, click **Simulation -> Options**

1. Under **Plane Void Meshing**, click radial button for **Automatically determine which voids to mesh**
2. Under **Trace Coupling**
   - Trace Coupling Distance: 10 mils
   - Min Coupled Trace Length: 10 mils
   - Only consider signal traces during coupling analysis: ☑ Checked
3. Under **Solver**, set the number of CPUs if you have SIwave multi processor license
4. Under **Mesh Refinement**, click radial button for **Automatic**
5. Under **Boundary Condition to Use**, click radial button for **Open Boundary**
6. Ignore nets named “DUMMY” or “Unused” during Simulation: ☑ Checked
7. Perform ERC during simulation setup: ☑ Checked
8. Click OK to exit
Changing the View

Toolbar

- Pan
- Zoom in
- Fit All
- Rotate
- Dynamic Zoom
- Zoom Out
- Top-down View

Shortcuts

Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:

- **ALT + Drag** - Rotate
  - In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.

- **Shift + Drag** - Pan

- **ALT + Shift + Drag** - Dynamic Zoom
Define Ports on Signal Nets on the Solder Balls Side

- We are going to create ports p1 and p2 on nets PART_FREE_INIT and TXD_12_0__DLL_LTC respectively, on the solder ball side first.
- There are 2 ways to create port in SIwave, the user can use the mouse cursor to specify where to place the port, or use the automatic port generation feature to place the port at component pin or grouped pin location.
- We are going to use the automatic port generation feature in this example.

To create port p1 with the automatic port generation feature:

1. Select Edit -> Generate Circuit Elements
2. Part name: BGA
   - This means we will be working on pins that are on a part called BGA, which is the solder balls side.
3. Reference Designator : P1
   - For PCB and stacked die application, you will have multiple instances of the same part, make sure you select the right reference designator here.
4. Select PART_FREE_INIT from the Circuit Element Positive Terminal listing.
   - Since there is only one pin, D5, connected to this net on part BGA.
   - It is sufficient to just select the net name. You need to select the pin you want to use if there are more than one pin listed.
5. Select GND from the Circuit Element Negative Terminal listing.
   - Expand GND to see all the pin listing, do not select any of them.
   - Select the pin name if you know which one you want to use as reference.
   - We are going to let SIwave to find the nearest GND pin from pin D5 and use that as a reference for the port we are going to create.
6. Click radial button for Use nearest pin as reference pin.
7. Circuit Element Type: Port.
8. Click on Create.
   - A port named P_P1_D5_1 has just been created between PART_FREE_INIT and GND.
   - Expand Ports under Circuit Elements column, you will see port P_P1_D5_1 is listed there.
To rename port `P_P1_D5_1` to `p1`:

1. Highlight `P_P1_D5_1` under **Ports** in **Circuit Elements** column
2. Click **Edit Selection**
3. Change the name to `p1`
4. Click **OK**
5. Expand **Ports** under **Circuit Elements** column, you will see the new port name is `p1`
To create port p2 on net TXD_12_0__DLL_LTC:
1. Select TXD_12_0__DLL_LTC from the Circuit Element Positive Terminal listing
   - Since there is only one pin, C4, connected to this net on part BGA. It is sufficient to just select the net name. You need to select the pin you want to use if there are more than one pin listed
2. Select GND from the Circuit Element Negative Terminal listing
   - Expand GND to see all the pin listing, do not select any of them
   - Select the pin name if you know which one you want to use as reference
   - We are going to let SIwave to find the nearest GND pin from pin C4 and use that as a reference for the port we are going to create
3. Click radial button for Use nearest pin as reference pin
4. Circuit Element Type: Port
5. Click on Create
   - A port named P_P1_C4_1 has just been created between TXD_12_0__DLL_LTC and GND
   - Expand Ports under Circuit Elements column, you will see the new port P_P1_C4_1 is listed there
6. Highlight P_P1_C4_1 under Ports in Circuit Elements column
7. Click Edit Selection
8. Change the name to p2
9. Click OK
Define Ports on Signal Nets on the Bond Wires Side

With ports p1 and p2 created, we are going to create ports p3 and p4 on nets PART_FREE_INIT and TXD_12_0__DLL_LTC respectively, on the bond wires side.

To create port p3 on net PART_FREE_INIT:

1. Part name: DIE
   - This means we will be working on pins that are on a part called DIE, which is the bond wires side.
2. Reference Designator: D1
   - For PCB and stacked die application, you will have multiple instances of the same part, make sure you select the right reference designator here.
3. Select PART_FREE_INIT from the Circuit Element Positive Terminal listing
   - Since there is only one pin, 290, connected to this net on part DIE. It is sufficient to just select the net name. You need to select the pin you want to use if there are more than one pin listed
4. Select GND from the Circuit Element Negative Terminal listing
   - Expand GND to see all the pin listing, do not select any of them
   - Select the pin name if you know which one you want to use as reference
   - We are going to let SIwave to find the nearest GND pin from pin 290 and use that as a reference for the port we are going to create
5. Click radial button for Use nearest pin as reference pin
6. Circuit Element Type: Port
7. Click on Create
   - A port named P_D1_290_1 has just been created between PART_FREE_INIT and GND
   - Expand Ports under Circuit Elements column, you will see the new port P_D1_290_1 is listed there
8. Highlight P_D1_290_1 under Ports in Circuit Elements column
9. Click Edit Selection
10. Change the name to p3
11. Click OK
To create port p4 on net TXD_12_0__DLL_LTC:

1. Part name: DIE
   - This means we will be working on pins that are on a part called DIE, which is the bond wires side.

2. Reference Designator: D1
   - For PCB and stacked die application, you will have multiple instances of the same part, make sure you select the right reference designator here.

3. Select TXD_12_0__DLL_LTC from the Circuit Element Positive Terminal listing
   - Since there is only one pin, 289, connected to this net on part DIE. It is sufficient to just select the net name. You need to select the pin you want to use if there are more than one pin listed

4. Select GND from the Circuit Element Negative Terminal listing
   - Expand GND to see all the pin listing, do not select any of them
   - Select the pin name if you know which one you want to use as reference
   - We are going to let SIwave to find the nearest GND pin from pin 289 and use that as a reference for the port we are going to create

5. Click radial button for Use nearest pin as reference pin

6. Circuit Element Type: Port

7. Click on Create
   - A port named P_D1_289_1 has just been created between TXD_12_0__DLL_LTC and GND
   - Expand Ports under Circuit Elements column, you will see the new port P_D1_289_1 is listed there

8. Highlight P_D1_289_1 under Ports in Circuit Elements column

9. Click Edit Selection

10. Change the name to p4

11. Click OK
Click **OK** to exit **Circuit Element Generation Dialog** window

**Verify Ports**

To Verify the ports we just created exist and we didn’t make mistake in terminal connections

1. Click **Edit -> Circuit Element Parameters**
2. Click on **Ports** tab
3. Verify that ports **p1**, **p2** **p3** and **p4** have the right reference impedance, port positive and negative nets and terminals
4. Click **OK** to exit **Circuit Element Properties** window

**View Ports Graphically**

To view ports graphically

1. Rotate the layout to have solder balls face up
2. Zoom in to the region where ports p1 and p2 are defined
3. To toggle off the simplify circuit elements display
   
   ![Simplify Circuit Elements](image)

   Select **View -> Simplify Circuit Elements**

4. To turn on the port name display
   
   ![Show Circuit Elements](image)

   Select **View -> Circuit Elements -> Element Names -> Ports**

5. To change the color of GND net so that the negative reference pin can be easily identified
   
   ![Change Net Color](image)

   - Click the **Nets** tab
   - Highlight net **GND**
   - Right mouse click and select **Change Net Color**
   - Click on a green color from the color template, and click **OK**
Computing S-Parameters

To compute the s-parameters:

1. Select **Simulation -> Compute S-, Y-, Z-Parameters**

   - Change the settings to as shown below

2. Click **OK** to start the simulation

3. When the simulation is completed, **SIwave Reporter** will be launched automatically with the s-parameter plots loaded
Create New Plot in SIwave Reporter

To create new plot:

1. Select SIwave -> Results -> Create Report
2. Click OK
3. Hold down CTRL key on the keyboard, select \textit{S(p1,p1)}, \textit{S(p1,p3)}, \textit{S(p2,p2)} and \textit{S(p2,p4)}
4. Click Add Trace
5. Click Done

These are the insertion and return losses for nets \textit{PART\_FREE\_INIT} and \textit{TXD\_12\_0\_DLL\_LTC}

\begin{figure}
\centering
\includegraphics[width=\textwidth]{plot.png}
\caption{Example - Package S-parameters}
\end{figure}

\begin{itemize}
\item When done viewing the \textbf{S-Parameters}, select File -> Exit
\item Click Yes to save the changes
\end{itemize}
Save SIwave Project

To save SIwave project:
1. Select *File -> Save As*
2. File name: *bga_s-para*
3. Click *Save*

Export Touchstone File

To export Touchstone file:
1. Select *Results -> S-, Y-, Z-Parameters -> Export to Touchstone (R) File*
2. Filename: *bga_s-para*
3. Click *Save*
4. Click *OK* to accept the 50 ohms renormalization

Touchstone file *bga_s-para.s4p* is created in the working directory
Ansoft Designer - Crosstalk Simulation

Launching Ansoft Designer

To access Ansoft Designer, click the Microsoft Start Button, select All Programs -> Ansoft -> Designer v3 -> Ansoft Designer 3

Creating a New Circuit

To create a new circuit:

1. From the Project menu, select Insert Circuit Design.
2. Click None button when prompted for Choose Layout Technology

Note: In this example we are not creating a layout or using components such as transmission lines that require substrate or stack up information. If we did, then it is recommended to choose a stack up from the list or create your own.

Project Manager Window
Creating the Circuit

Component Placement

Importing S-parameters
1. Select the menu item **Draw -> N-Port** or click the toolbar button.
2. In the N-port data window,
   - Select the **Link to file** radial button
   - Click the browse button to locate and select your Touchstone file: `bga_s-para.s4p`
   - Click the **Open** button
3. Click the **OK** button
Component Placement - continued

- To place the new component, single click with the left mouse button in the middle of the screen.
- Press the space bar to finish the placement.

Placing Resistors, Voltage Sources, and Voltage Probes

1. Click the **Components** tab in the **Project Manager** window.
   - **Resistors**: Expand **Lumped** -> **Resistors**
   - **Voltage Sources**: Expand **Sources** -> **Independent Sources**
   - **Voltage probes**: Expand **Probes**
Component Placement - continued

Place 4 Resistors in the schematic

1. In the Components Tab, under Lumped -> Resistors, double click RES: Resistor
2. Click the left mouse button 4 times to place 4 resistors in the schematic
3. To end the placement, click the right mouse button and select Finish. (You can also end the placement by pressing the space bar or Esc)

Note: Before placing a component on the schematic use the R key to rotate. If a component is already placed, use the <CTRL> R key to rotate.

Change the value of the resistors

1. Right mouse click the component and then select Properties in the pull down menu
2. Change the value from 100 to 50, then click OK

Note: alternatively, you can double left mouse click on the resistor to bring up the Properties window (shown below) and change the value from 100 to 50, then hit OK
Component Placement - continued

Place Pulse Source
1. In the Components Tab, under Sources -> Independent Sources, double click on VDC:Voltage Source.
2. Left mouse click to place the source in the schematic
3. Press the space bar to finish the placement

Define Pulse Source
1. Right mouse click the source component and then select Edit Source in the pull down menu
2. For Name type Vs
3. For Type, choose Pulse (time points)
4. Enter the pulse properties as show below
5. Click OK
Component Placement - continued

Adding Wiring to connect components
1. Select the menu item Draw -> Wire
2. Place the cursor (which is now an X) over a node and left mouse click once
3. Drag the mouse to the connection node and left mouse click once.
4. Repeat this procedure until the connections below are made

Adding Ground Connections
1. Select the menu item Draw -> Ground (alternatively you can select the toolbar icon)
2. Place 1 ground connection on the end of the voltage source, and 3 ground connections on the ends of the 3 resistors

Adding Voltage Probes
1. In the Components tab, expand the Probes, double click on VPRB: Voltage Probe
2. Using the left mouse button to place 4 voltage probes in the schematic and name them Vin1, Vout1, Vxtk1, and Vxtk2
Save Project

To save the project:
1. In the Ansoft Designer window, select the menu item File -> Save As
2. From the Save As window, type the Filename: bga_xtalk
3. Click the Save button

Analysis Setup

To create an analysis setup:
1. Select the menu item Circuit -> Add Solution Setup
2. Analysis Setup Window:
   - For Analysis Type, choose Transient Analysis
   - Click Next
   - Analysis Control
     1. Length of Analysis: 20ns
     2. Maximum Time Step Allowed: 0.1ns
   - Convolution Control
     1. Maximum Sampling Frequency: 10GHz
     2. Delta Frequency: 0.01GHz
   - Click Finish
3. Select the menu item Circuit -> Analyze
Plot Input, Output and Crosstalk Waveforms

To create a report:
1. Select the menu item *Circuit -> Create Report*
2. Create Report Window:
   - Report Type: *Standard*
   - Display Type: *Rectangular Plot*
   - Click the OK button
3. Traces Window:
   - Category: *Voltage*
   - Quantity: V(VPRB:Vxtk1), V(VPRB:Vout1), V(VPRB:Vin1), and V(VPRB:Vxtk2)
   - Function: *<none>*
   - Click the Add Trace button
   - Click the Done button

When done viewing the waveforms, select *File -> Exit*
Click *Yes* to save the changes
**Compute Differential S-parameters**

- Nets **PART_FREE_INIT** and **TXD_12_0__DLL_LTC** are not differential nets, but let’s assume they are differential nets so that we can show you how to obtain differential S-parameters.

To compute differential S-parameters:

1. Select **Simulation -> Compute Differential S-, Y-, Z-Parameters**
2. To define differential port on the balls side:
   - Positive Reference Port: **p1**
   - Negative Reference Port: **p2**
   - Click **Create Differential Pair** button
   - Enter differential pair name: **d1**
   - Click **OK** button
3. To define differential port on the bond wires side:
   - Positive Reference Port: **p3**
   - Negative Reference Port: **p4**
   - Click **Create Differential Pair** button
   - Enter differential pair name: **d2**
   - Click **OK** button

4. Click **Plot** button
To create new differential S-parameters plot:
1. In the **SIwave Reporter** window, select **SIwave -> Results -> Create Report**
2. Click **OK** button
3. Hold down **CTRL** key on the keyboard, select St(d1:Diff,d1:Diff), St(d1:Diff,d2:Diff), St(d2:Diff,d1:Diff) and St(d2:Diff,d2:Diff)
4. Click **Add Trace**
5. Click **Done**

When done viewing the **Differential S-Parameters**, select **File -> Exit**
Click **Yes** to save the changes
Click **OK** to exit Compute Differential S-, Y-, Z-Parameters window in SIwave main GUI
Creating a Full Wave Spice Subcircuit

To create a FWS subcircuit:
1. Select Simulation -> Compute FWS sub-circuit
2. File name: bga_nets
   By default the file will be saved in the project directory
3. Full Wave SPICE Subcircuit Format: HSPICE
4. Use common ground for Spice output: ✔ Checked
5. Click OK

6. Click Close when the Full-wave Subcircuit window comes up
   HSPICE subcircuit bga_nets.sp is created in the project directory
Creating a Lumped RLGC Subcircuit

To create a lumped RLGC matrices:
1. Select **Simulation -> Compute RLGC sub-circuit**
   - Compute RLGC Parameters at: 2.004e+007Hz
   - Click **Auto Assign Source/Sink Terminals**
   - Select all items in the table listing
2. Click **Compute RLGC Matrices**
   - A window as shown below will come up
   - Click on the appropriate tab to see R, L, G, or C matrix

   ![RLGC Matrices window](image)

<table>
<thead>
<tr>
<th>Resistance (Ohm)</th>
<th>Inductance (nH)</th>
<th>Capacitance (pF)</th>
<th>Conductance (mS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PART_FREQ_INT:1p1</td>
<td>TXD_1:0__DNL:LC:1p2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.95067e-001</td>
<td>8.05590e-002</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXD_1:0__DNL:LC:1p2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.95099e-002</td>
<td>3.15010e-003</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To create a lumped RLGC subcircuit:
1. Click **Export RLGC Subcircuit**
   - Subcircuit Format: **HSPICE**
   - Output File Name: **bga_nets_lumped**
   - Number of Lumps: **5**
2. Click **OK**
   - Lumped subcircuit **bga_nets_lumped.sp** is created
3. Click **Close** button on the **RLGC Matrices** window
4. Click **OK** to exit **Compute RLGC Sub-Circuit** window
Example - Package S-parameters

△ Save SIwave Project
   △ To save SIwave project:
       1. Select File -> Save

△ Exit SIwave
   △ Select File -> Exit
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SSN Simulation

The example is intended to show you how to simulate SSN. Two signal nets will be driven and 1 signal net will be left quiet. We will look at the noise on the quiet signal net and power rail.
You will learn how to:
1. Create ports using automatic port generation feature
2. Compute S-parameters
3. Compute FWS subcircuit
4. Import IBIS model for time domain simulation
5. Simulate SSN with FWS subcircuit using NEXXIM and Ansoft Designer
Ansoft SIwave Design Environment

The following features of the Ansoft SIwave Design Environment are used to create this passive device model:

- Pre-processing
  - Automatic ports generation
- Boundaries/Sources
  - Ports
  - IBIS drivers and receivers
- Solutions
  - S-Parameters
  - SSN (transient) simulation with Ansoft Designer and NEXXIM
- Plots
  - S-Parameter sweep
  - Time domain waveforms
- Export
  - Full Wave Spice subcircuit
Open a SIwave Project

- Click the Microsoft **Start** Button, select **All Programs -> Ansoft -> SIwave3** -> **SIwave 3** program.
- This will bring up SIwave3 window with empty project
- Click **File -> Open**, browse to the folder that contains **siwave_ch5_ssn.siw**, select **siwave_ch5_ssn.siw**, and click **Open**.
Validation Check

It is a good idea to do a validation check before you start working on any design in SIwave for the first time.

The Validation Check consists of self-intersecting polygons, disjoint nets, overlapping nets (dc-shorted) and nets with overlapping vias checks.

The last thing you want to find out is that you need a new layout after all the settings and ports have been defined.

To do a validation check:

1. Select Edit -> Validation Check
2. Click Start button to start the validation
3. When the validation is completed, you should see a window like below

4. There is no layout and DRC related problem with this design. Net names will be listed in the message window if there are any problems.
5. Click Close to exit the Validation Check window.
Changing the View

Toolbar

Pan  Zoom in  Fit All

Rotate  Tab

Dynamic Zoom  Zoom Out

Top-down View

Shortcuts

Since changing the view is a frequently used operation, some useful shortcut keys exist. Press the appropriate keys and drag the mouse with the left button pressed:

- **ALT + Drag** - Rotate
  - In addition, there are 9 pre-defined view angles that can be selected by holding the ALT key and double clicking on the locations shown on the next page.

- **Shift + Drag** - Pan

- **ALT + Shift + Drag** - Dynamic Zoom

Predefined View Angles

Top  Left  Right

Bottom
Searching for Component and Pin Names

The goal of this example is to drive nets \( \text{ST\_DATA1} \) and \( \text{ST\_DATA2} \) with a stimulus, then observe noise on net \( \text{ST\_DATA3} \) and \( \text{VCC} \), with respect to \( \text{GND} \).

Ports are needed on \( \text{ST\_DATA1} \), \( \text{ST\_DATA2} \), \( \text{ST\_DATA3} \), and \( \text{VCC} \), with \( \text{GND} \) as the negative reference net.

In order to make port creating easier, we need to find out what components are connected to these nets, and what are their pin names.

Click on the \textit{Nets} tab
1. \( \text{ST\_DATA1}: \checkmark \text{Checked} \)
2. \( \text{ST\_DATA2}: \checkmark \text{Checked} \)
3. \( \text{ST\_DATA3}: \checkmark \text{Checked} \)

Zoom in to the highlight nets area

Toggle ON the pin names display
1. Select \textit{View -> Circuit Elements -> Pin Names -> All On}.

Change VCC net color to red
1. Highlight net \( \text{VCC} \)
2. Right mouse click and select \textit{Change Net Color}
3. Click on a red color from the color template, and click \textit{OK}.

Change GND net color to green
1. Highlight net \( \text{GND} \)
2. Right mouse click and select \textit{Change Net Color}
3. Click on a green color from the color template, and click \textit{OK}.

Change the top layer from wire frame to solid color display
1. Click on the \textit{Layers} tab
2. Click on the color box net to \textit{SURFACE}.
The 3 signal nets are highlighted in yellow, VCC pins are in red and GND pins are in green.

The 3 signal nets are connected to component U27 and U37.

ST_DATA1 is connected to pins U27-12 and U37-4.

ST_DATA2 is connected to pins U27-11 and U37-15.

ST_DATA3 is connected to pins U27-10 and U37-5.

VCC pins are U27-28 and U37-20.

GND pins are U27-14 and U37-10.
Searching for Component and Pin Names - continued

You can also verify the above pins info by using the Circuit Elements tab

1. Click on Circuit Elements tab
2. Expand Integrated Circuits
3. Expand 74ACT299_SOIC
4. Expand U37

![Circuit Elements](image-url)
5. Expand **PAL22V10_SMSOCKETAMD**
6. Expand **U27**

```
PAL22V10_SMSOCKETAMD
+ R U16
+ R U17
+ R U27
   1 (DUMMY)
   2 (CLK_125K)
   3 (TSD_RST_N)
   4 (ST_EN_N)
   5 (ST_DATA7)
   6 (ST_DATA6)
   7 (ST_DATA5)
   8 (DUMMY)
   9 (ST_DATA4)
  10 (ST_DATA3)
  11 (ST_DATA2)
  12 (ST_DATA1)
  13 (ST_DATA0)
  14 (GND)
  15 (DUMMY)
  16 (UN122V1023P1IN130)
  17 (P_TLV_ERR)
  18 (R_TLV_ERR)
  19 (P_DIG1_POWER_STATUS)
  20 (R_DIG1_POWER_STATUS)
  21 (P_DIG2_POWER_STATUS)
  22 (DUMMY)
  23 (R_DIG2_POWER_STATUS)
  24 (P_DIG3_POWER_STATUS)
  25 (R_DIG3_POWER_STATUS)
  26 (P_FIFO_POWER_STATUS)
  27 (R_FIFO_POWER_STATUS)
  28 (VCC)
 NC1 (DUMMY)
 NC2 (DUMMY)
```
### Automatic Ports Generation

To create ports on component U27:

1. Click on the **Circuit Elements** tab
2. Expand **Integrated Circuits**
3. Expand **PAL22V10_SMSOCKETAMD**
4. Expand U27
5. Hold down **CTRL** key on the keyboard, select pins **10, 11, 12** and **28**
6. Right mouse click in the **Circuit Elements** tree, select **Create Port(s)**
7. In the **Choose reference pin window**:
   - Part Type: **PAL22V10_SMSOCKETAMD**
   - Reference Designator: **U27**
   - Select **14 (GND)** for the pin number
   - Click **OK**
8. You can see in the display area that 4 ports are added to component U27
**Automatic Ports Generation - continued**

To create ports on component U37

1. Click on the **Circuit Elements** tab
2. Expand **Integrated Circuits**
3. Expand **74ACT299_SOIC**
4. Expand **U37**
5. Hold down **CTRL** key on the keyboard, select pins **4, 5, 15** and **20**
6. Right mouse click in the **Circuit Elements** tree, select **Create Port(s)**
7. In the **Choose reference pin window:**
   - **Part Type:** **74ACT299_SOIC**
   - **Reference Designator:** **U37**
   - Select **10 (GND)** for the pin number
   - Click **OK**
8. You can see in the display area that 4 ports are added to component U37
Create Port for VRM

We need a port for external power supply, and we want this port to be at the edge of the PCB.

Zoom in to the bottom left corner of the design, we are going to create a port on connector J3 between pins 1 and 3 manually.

To create port manually:

1. Select **Circuit Elements -> Ports**
2. Place mouse cursor on top of pin 1 of connector J3, do a left mouse click when round bull eye mouse cursor appears
3. Place mouse cursor on top of pin 3 of connector J3, do a left mouse click when round bull eye mouse cursor appears
4. In the **Select layers for port terminals** window:
   - Positive Terminal Resides on Layer: **SURFACE VCC**
   - Negative Terminal Resides on Layer: **SURFACE GND**
   - Click **OK**
5. In the **Port Properties** window:
   - Name: **VRM**
   - Reference Impedance: **50 Ohms**
   - Click **OK**
Verify Ports

To verify the ports we just created exist and we didn’t make mistake in terminal connections:

1. Click **Edit -> Circuit Element Parameters**
2. Click on **Ports** tab
3. Verify that all 9 ports have the right reference impedance, port positive and negative nets
4. Click **OK** to exit **Circuit Element Properties** window

![Circuit Element Properties](image)
Setting Simulation Global Options

In the Silwave menu bar, select **Simulation -> Options**

1. Under **Solver**, set to the correct number of CPUs if you have Silwave multi-processor license
2. Change the rest of the settings to as shown below

3. Click **OK** to exit

By default, Silwave meshes at the highest frequency of the sweep. One can overwrite the default mesh frequency by specifying a mesh frequency in the window as shown above.
Computing S-Parameters

To compute the s-parameters:

1. For Full Wave Spice export, we would run the frequency sweep up to the knee frequency \( F_{knee} \), where \( F_{knee} \approx 0.5/rise\_time \).
2. For a 100 ps rising edge source, the knee frequency is 5 GHz
3. Select *Simulation -> Compute S-, Y-, Z-Parameters*
   - Change the settings to as shown below

![Image of SIwave GUI showing Compute S-, Y-, Z-parameters/FWS Circuit]

4. Click **OK** to start the simulation

5. When the simulation is completed, **SIwave Reporter** will be launched with the s-parameter plots loaded

   - When done viewing the **S-Parameters**, select **File -> Exit**
   - Click **Yes** to save the changes if prompted
Save Siwave Project

To save Siwave project:
1. Select File -> Save As
2. File name: ssn
3. Click Save

Creating a Full Wave Spice Subcircuit

To create a FWS subcircuit:
1. Select Simulation -> Compute FWS sub-circuit
2. File name: ssn
   - By default the file will be saved in the project directory
3. Full Wave SPICE Subcircuit Format: Nexxim
4. Launch Designer Nexxim: ✔ Checked
5. Click OK

Click Close when the Full-wave Subcircuit window comes up
Ansoft Designer is launched with ssn subcircuit loaded
**Creating the Circuit**

1. Select **Tools -> Import SPICE Components**
2. File of Type: IBIS FILE (*.ibs)
3. Browse to folder which contains **pproibis.ibs**, select **pproibis.ibs** and click Open
4. Click **Deselect All**
5. **pproibis_GTL_IN**: ☑ Checked
6. **pproibis_GTL_OUT**: ☑ Checked
7. Click OK

**Component Placement**

**Importing IBIS models**
Component Placement - continued

Imported IBIS driver and receiver are available under **Components** tab
Component Placement - continued

Place IBIS drivers
1. Click the **Components** tab in the **Project Manager** window.
2. Double click on **proibis_GTL_OUT**
3. Using the left mouse button to place 3 IBIS drivers in the schematic
4. Press the **space bar** to finish the placement

Place Pulse Source
1. In the Components Tab, under **Independent Sources**, double click on **V_PULSE: Pulse Voltage Source**.
2. Left mouse click to place the source to the bottom left corner in the schematic. This is the source for the IBIS driver input.
3. Press the **space bar** to finish the placement
Component Placement - continued

Define Pulse Source

1. Right mouse click the source component and then select **Properties** in the pull down menu
2. Enter the pulse properties as show below
3. Click **OK** when done

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACMAG</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>ACM-ISE</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>DC</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>V2</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>TD</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>TR</td>
<td>500</td>
<td>ps</td>
</tr>
<tr>
<td>TF</td>
<td>500</td>
<td>ps</td>
</tr>
<tr>
<td>PW</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>PER</td>
<td>40</td>
<td>ns</td>
</tr>
</tbody>
</table>

Add Ground

1. Select the menu item **Draw -> Ground** (alternatively you can select the toolbar icon)
2. Place 1 ground connection on the end of the voltage source, and 3 ground connections on the **GND** terminals of the IBIS drivers

Add Wiring to connect components

1. Select the menu item **Draw -> Wire**
2. Place the cursor (which is now an X) over a node and left mouse click once
3. Drag the mouse to the connection node and left mouse click once.
4. Repeat this procedure until the connections on the next page are made
Component Placement - continued

Place IBIS receivers

1. Click the Components tab in the Project Manager window.
   - Double click on pproibis_GTL_IN
   - Using the left mouse button to place 3 IBIS receivers in the schematic
   - Press the space bar to finish the placement
Component Placement - continued

Place DC Source
1. In the Components Tab, under Independent Sources, double click on V_DC: DC Voltage Source.
2. Left mouse click to place the source to the bottom right corner in the schematic. This will be connected to the VRM terminal later.
3. Press the space bar to finish the placement

Define DC Source
1. Right mouse click the source component and then select Properties in the pull down menu
2. Enter 1.5V for the DC voltage
3. Click OK when done

<table>
<thead>
<tr>
<th>Name</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Mag</td>
<td>nan</td>
</tr>
<tr>
<td>AC Phase</td>
<td>0</td>
</tr>
<tr>
<td>DC</td>
<td>1.5</td>
</tr>
<tr>
<td>Status</td>
<td>Active</td>
</tr>
<tr>
<td>Info</td>
<td>V_DC</td>
</tr>
</tbody>
</table>

Add Ground
1. Select the menu item Draw -> Ground (alternatively you can select the toolbar icon)
2. Place 1 ground connection on the end of the DC voltage source, and 3 ground connections on the GND terminals of the IBIS receivers

Add Wiring to connect components
1. Select the menu item Draw -> Wire
2. Place the cursor (which is now an X) over a node and left mouse click once
3. Drag the mouse to the connection node and left mouse click once.
4. Repeat this procedure until the connections on the next page are made
Component Placement - continued

Define receivers bias
1. Add resistors
   - In the Components Tab, under Resistors, double click RES: Resistor
   - Click the left mouse button 3 times to place 3 resistors in parallel at the top right corner of the schematic
   - To end the placement, click the right mouse button and select Finish. (You can also end the placement by pressing the space bar or Esc)
Component Placement - continued

2. Change the value of the resistors
   - Right mouse click the component and then select Properties in the pull down menu
   - Change the value 25, then click OK
   - Note: alternatively, you can double left mouse click on the resistor to bring up the Properties window (shown below) and change the value to 25, then click OK

3. Add DC bias voltage
   - We are going to copy the DC source we defined for the VRM earlier
   - Select the DC Source and the ground that is connect to it
   - Select Edit -> Copy
   - Select Edit -> Paste, place the DC source and ground to the right side of the 3 resistors with left mouse click

Add Wiring to connect components

1. Select the menu item Draw -> Wire
2. Place the cursor (which is now an X) over a node and left mouse click once
3. Drag the mouse to the connection node and left mouse click once.
4. Repeat this procedure until the connections on the next page are made
Component Placement - continued

Adding Voltage Probes

1. In the Components tab, expand the Probes, double click on VPROBE: Voltage Probe
2. Using the left mouse button to place 8 voltage probes in the schematic and name them logic_in, VRM, ST_DATA1_in, ST_DATA1_out, ST_DATA3_in, ST_DATA3_out, VCC_U27 and VCC_U37

Save Project

To save the project:
1. In the Ansoft Designer window, select the menu item File -> Save As
2. From the Save As window, type the Filename: ssn
3. Click the Save button
**Analysis Setup**

To create an analysis setup:

1. Select the menu item **Nexxim Circuit -> Add Solution Setup**
2. Analysis Setup Window:
   - Analysis Type: **Transient Analysis**
   - Click **Next**
   - Analysis Control
     1. Step: **0.1 ns**
     2. Stop: **40 ns**
   - Click **Finish**

3. Select the menu item **Nexxim Circuit -> Analyze**
Plot Input, Output and SSN Waveforms

To create a report:
1. Select the menu item **Nexxim Circuit → Create Report**
2. Create Report Window:
   - Report Type: **Standard**
   - Display Type: **Rectangular Plot**
   - Click the OK button
3. Traces Window:
   - Category: **Voltage**
   - Quantity: V(ST_DATA1_in), V(ST_DATA1_out), V(ST_DATA3_in), V(ST_DATA3_out), V(VCC_U27), and V(VCC_U37)
   - Function: <none>
   - Click the **Add Trace** button
   - Click the **Done** button
### What Do Those Waveforms Represent?

- **V(ST_DATA1_out):** Driver output signal on net ST_DATA1
- **V(ST_DATA1_in):** Receiver input signal on net ST_DATA1
- **V(ST_DATA3_out):** Noise on driver pin on net ST_DATA3 when nets ST_DATA1 and ST_DATA2 switched simultaneously
- **V(ST_DATA3_in):** Noise on receiver pin on net ST_DATA3 when nets ST_DATA1 and ST_DATA2 switched simultaneously
- **V(VCC_U27):** Voltage difference between VCC and GND on component U27, it is used to power the IBIS drivers
- **V(VCC_U37):** Voltage difference between VCC and GND on component U37, it is used to power the IBIS receivers

### Exit Ansoft Designer

- When done viewing the waveforms, select **File -> Exit**
- Click **Yes** to save the changes

### Save SIwave Project

- To save SIwave project:
  1. Select **File -> Save**

### Exit SIwave

- Select **File -> Exit**
Package on PCB Simulation

This example shows you how to connect a package onto a PCB for system level simulation.

You will learn how to:

1. Place a package onto a PCB design.
Ansoft SIwave Design Environment

The following features of the Ansoft SIwave Design Environment are used to create this passive device model

- Pre-processing
  - Merging a package design with a PCB design
Open the PCB Project

- Click the Microsoft *Start* Button, select *All Programs* -> *Ansoft* -> *Slwave 3* -> *Slwave 3* program.
- This will bring up Slwave3 window with empty project
- Click *File* -> *Open*, browse to the folder that contains *siwave_ch6_pcb.siw*, select *siwave_ch6_pcb.siw*, and click *Open*.

This is a 4-layer PCB, the package foot print is at the center of the PCB. We will place a 4-layer package at that location.
Open the Package Project

- Click \textit{File} -> \textit{Open}, browse to the folder that contains \texttt{siwave\_ch6\_package.siw}, select \texttt{siwave\_ch6\_package.siw}, and click \textit{Open}.

This is a 4-layer package, which will be placed onto the PCB.

Exit SIwave

- To exit SIwave:
  1. Select \textit{File} -> \textit{Exit}
Launch Package/PCB Merge Utility

To launch the utility:
1. Bring up a Windows Explorer from the Windows Start menu
2. Browse to the Ansoft/siwave3 folder located in the installation folder
3. Double click pkgonpcb.exe

This launches the Package/PCB Merge Utility

This utility takes either Slwave projects or ANFs as input, the output is going to be the same type as the input
**Merge the Package onto the PCB**

To merge the package onto the PCB:

1. Under Package Path:, click **Browse**, browse to the folder that contains `siwave_ch6_package.siw`, select `siwave_ch6_package.siw`, and click **Open**.
2. Under PCB Path:, click **Browse**, browse to the folder that contains `siwave_ch6_pcb.siw`, select `siwave_ch6_pcb.siw`, and click **Open**.
3. Under Merged Layout Path:, click **Browse**, browse to the working directory, enter `packageonpcb`, and click **Open**.
4. Under Locate Solderballs at Package Padstack, select **BBALL600**.
5. Enter the parameters as shown below.

---

### Package Placement Parameters

- **Package appears to have 282 pins**
- **Package x-offset:** 4530 mls
- **Package y-offset:** 7066 mls
- **Package rotation:** 0 degrees

**Package will be placed on TOP of the PCB**

- **Generate Solderballs**
- **Merge Nets**
  - **Net Merge Options**
    - Preserve PCB net names
    - Preserve package net names

### Solderball Parameters

- **Height:** 10 mls
- **Radius:** 5 mls

**Locate Solderballs at Package Padstack**

- **EBALL600**

---

6. Click **Execute Merge** to merge the 2 designs, `packageonpcb.siw` is created.
7. Click **Close**.
Open the Package on PCB Slwave Project

- Click the Microsoft *Start* Button, select *All Programs* -> *Ansoft* -> *Slwave 3*.
- Click *Slwave 3* program.
- This will bring up Slwave3 window with empty project.
- Click *File* -> *Open*, browse to the folder that contains `packageonpcb.siw`, select `packageonpcb.siw`, and click *Open*.

You can see that this is a 8-layer design now from the **Layers** tab of the GUI.

You can do all the things that are described in chapter 1 to 5 with this merged design.
Example - Package on PCB

Δ Save SIwave Project
  △ To save SIwave project:
    1. Select *File -> Save*

Δ Exit SIwave
  △ To exit SIwave:
    1. Select *File -> Exit*