Each problem is worth 20pts. Give all explanations, equations, and clearly explain your answers. Poorly explained answers will get 0pts. Do not collaborate, this is an individual test. Submit your report in SacCT. Good luck! Please clearly label all answers according to questions below:

1. **(25pts)** A 25cm, 10 GHz microstrip transmission line is fabricated on the Rogers 6006 substrate whose width is equal to the substrate height. Pick a standard height of the substrate from Rogers Laminate Guide. Students working in the same group should ensure they do not have the same thickness.
   
   (a) Calculate the impedance of this line, using Matlab and appropriate equations, then find the impedance of the line using LineCalc. How do they compare?
   
   (b) Calculate the electrical length of this line at 0.1 GHz using equations and Matlab, then using LineCalc. How do they compare?
   
   (c) Calculate the time-delay this line introduces using equations and Matlab. Calculate the time-delay using the electrical length found in LineCalc?
   
   (d) Using appropriate equations and Matlab calculate capacitance and inductance of the line, then calculate the time-delay that the line introduces.
   
   (e) Simulate this line in ADS in the time-domain. Terminate the line with an impedance that will prevent ringing, then find through simulations the time delay this line introduces. From these simulations can you find the simulated total capacitance and inductance of this line? How do these compare to the ones calculated previously? Can you calculate the bandwidth of this line?

2. **(25pts)** Using Matlab code described on the web site:
   
   http://www.mathworks.com/help/matlab/examples/square-wave-from-sine-waves.html
   
   Plot the exact and approximate waveforms using the dc component and first seven harmonics, then determine the bandwidths of the clock waveforms. Using the previous information plot the diagram Bandwidth vs. rise time diagram on a log-log scale.

3. **(25pts)** 800 m Pasternack flexible RG58CU coaxial cable, single shielded with black PVC jacket is given. Find the data sheet on pasternack.com for this cable. Find the dimensions of the inner and outer conductor. From this information find the inductance and capacitance of the cable per unit length, and then transmission-line impedance of the cable. Compare the values you calculated with given values in the data sheet. This cable is used to connect driver and receiver in a building, however during installation, the cable was shorted somewhere in the building. A TDR shows that the short circuit is about 400 m away. A TDR sends a pulse 10 V and 6 µs long. If the input impedance of TDR is 150 Ω:
   
   (a) Sketch the bouncing diagram with four bounces, if the TDR sends the pulse at t=0.
(b) What will be the voltage at the input of the line after several seconds?
(c) Use ADS to simulate this line, and prove that your calculations are correct by comparing the diagrams obtained by hand-calculations and simulations.

4. (25pts)
(a) Explain what is rail droop or rail collapse. Why is the impedance of the PDS kept below a target value?
(b) How is that accomplished?
(c) Download "Surface Mount Ceramic Capacitor Products - AVX product guide". In this product guide find the loop inductance of an C0G (NP0) Dielectric Capacitor in a 0805 package. Specifically look in General Specifications then look at the Figure entitled:"Variation of Impedance with Cap Value Impedance vs. Frequency 0805 - C0G (NP0) 10 pF vs. 100 pF". Hint: If you are having trouble answering this question, look in Bogatin’s book section on The Power-Distribution Network and Loop Inductance, then think how he found the loop inductance of the 1 nH 0603 decoupling capacitor.
(d) If you want to use a 1000 pF capacitor as a decoupling capacitor in a circuit, how many capacitors in parallel do you have to have in order to keep the maximum loop inductance to 1/2 of the loop inductance of a single capacitor?

5. (25pts) Two CMOS drivers are connected by 2 in long, 10 mils wide microstrip line on a 47 mils glass-epoxy PCB substrate. The input capacitance of this CMOS driver is about 5 pF, and the output resistance of the driver is 10 Ω. The CMOS driver’s voltage is a 5 V, 50 MHz clock waveform having 50% duty cycle and 0.5 ns fall and rise times. Simulate this line using ADS and plot the voltages at the input and output of the line. At what times (if any) will the receiver CMOS (CMOS at the load side) produce false logic triggering? If the receiver is producing false logic triggering, provide the solution that will solve this problem. Finally, design an equivalent transmission-line circuit for the microstrip line. Show that the equivalent circuit can be placed instead of the transmission line between two CMOS drivers, and you will get the same voltages and the input and the output of the circuit. Hint: Note that you have some freedom in selecting specific FR4 substrate.

Don’t forget to also submit your individual homework in SacCT.