LOW POWER DESIGN
\[ i_{\text{supply}} = C_L \frac{dV}{dt} \]

where \( C_L \) is the load capacitance and \( V \) the instantaneous voltage across that capacitance. Now, if the supply voltage is \( V_{dd} \), then the instantaneous power being consumed in the circuit consisting of the gate and the capacitive load is given as

\[ P = i_{\text{supply}} V_{dd} = V_{dd} C_L \frac{dv}{dt} \]
Figure 11.12 Circuit Model for Power Dissipated in a CMOS Gate
Thus the power consumed for the circuit as a whole is given as

\[
\text{Power} = \sum_{\text{node}} N_{\text{node}} C_L V_{dd}^2 f_{\text{clock}}
\]

where \( f_{\text{clock}} \) is the clock frequency and \( N_{\text{node}} \) is the fraction of clock cycles that each node switches, hereafter referred as the switching activity.
reg [31:0] C;
reg [31:0] A, B;

always @(posedge clock)
  C <= A + B;
Figure 11.13 □ Potentially Power-Inefficient Multiplier Design
reg [31:0] C;
reg [15:0] A,B;
tri [15:0] Ain,Bin;
always @(posedge clock)
C = Ain + Bin

assign Ain = GoForthAndMultiply ? A : 16'hzzzz;
assign Bin = GoForthAndMultiply ? B : 16'hzzzz;
reg [31:0] C;
reg [15:0] A,B;
wire [15:0] Ain,Bin;

always @(posedge clock)
C = Ain + Bin

assign Ain = GoForthAndMultiply ? A : 16'h0;
assign Bin = GoForthAndMultiply ? B : 16'h0;
Figure 11.14 More Power-Efficient Multiplier design
reg [31:0] C;
reg [15:0] A,B;
wire [15:0] Ain,Bin;

always @(posedge clock)
begin
    C <= Ain + Bin
    if (GoForthAndMultiply == 1)
        begin
            Ain <= A;
            Bin <= B;
        end
end
1. Transistor and switch level: These can estimate the power to within a few percent of silicon but are limited to a few hundred devices at the transistor level (although more at a switch level) at the cost of long compute times. Such tools also have the disadvantage that power overruns will be revealed only after the design has progressed through layout and extraction.

2. Gate Level: Given a gate-level netlist in Verilog, VHDL, or EDIF and a gate-level library for power, these tools can incorporate the actual switching activities from a simulation testbench to produce power estimates to within 10-15 percent of silicon. Also at this power compliers are available which use expression factoring, technology mapping, cell sizing to achieve power reductions of 10-15 percent. Still designers would prefer information earlier in the design cycle.

3. Architectural and RTL: Statistical techniques for power estimation at the level is still an active area of research. Tools are starting to appear that link power estimates to source code in RTL-level Verilog or VHDL to within about 20-25 percent of silicon. It is also an order of magnitude faster than the gate level
wire [15:0] A,B,C;
wire [7:0] In1, In2 ,In3;
wire Multselect;

assign A = In1 + In2;
assign B = In1 + In3;
assign C = MultSelect ? A : B;