CSc/CpE 142
Advanced Computer Organization

Instructor: Dr. Behnam S. Arad
Phone: (916) 278-7160
Professor of Computer Science & Computer Engineering
Office: RVR 5044
Office Hours: Posted @ http://ecs.csus.edu/~arad
E-mail Address: arad@csus.edu

Required Text:

Optional Reference:

Grading Policy*:
- Term Project/Quizzes/Graded assignments 25%
- Exam 1 25%
- Exam 2 25%
- Final Exam 25%

*The necessary requirement to pass the course is to perform satisfactory in the term project. The term project requires typed reports and a demo that may be scheduled during the last week of classes. You may be required to turn in a project report during the last week of classes as well.

Course Description:
Design and performance issues of computers. Topics include instruction set architecture, computer arithmetic, processor design, survey of contemporary architectures, interfacing I/O devices, hierarchical memory design and analysis, parallelism and multiprocessing, distributed systems, techniques for enhancing performance, and an introduction to EDA tools for design and verification of computers. Students will design and simulate a microcomputer in an HDL. Cross-listed as CPE 142, and can be taken only once for credit.

Prerequisite:
CSC 137 (for CSC students), CPE 166 & CPE 185 (for CPE students).

Course Policies and Information:
1. Class attendance is required. Any adjustment to this syllabus or assignments will be announced in class. In addition, you must check your E-mail messages regularly for any important announcement distributed regarding this course.

2. Exams will be closed book/closed notes. Prior to each exam, review guidelines will be provided. No make-up exam will be arranged unless there is a serious and compelling
reason. The instructor must be notified prior to the exam, otherwise no make-up exam will be given.

3. Graded assignments should be submitted as one PDF file through SacCT. You can learn about SacCT submission by visiting http://www.csus.edu/sacct/. Each assignment should be typed and have a cover including the following information: Course number, Section, instructor, assignment number, due date, date submitted, and your name. Unless otherwise noted, late assignments submitted within one week of the due date will receive a %5 deduction. Late assignments will not be accepted once the solution has been provided.

Some assignments may require hardcopy submissions as well. This will be explicitly mentioned in the assignment. Hardcopy deliverables are due in the CSc main office (RVR 3018) by 4 pm on the due date. Time stamp the cover and drop the assignment in the CSC drop box (CPE/EEE students please use CSC drop box as well).

For certain assignments, only a subset of problems may be graded. The subset will not be announced in advance. You should complete all assigned problems.

4. You can use a laptop during the lecture only if it is used to take notes for this course. You should not use the system for other purposes during the lecture or in a manner that will disturb other students. All cell phones, pagers, and similar devices should be on a silent mode. **No Texting or surfing the internet during the lecture is allowed.**

5. If you do not already have one, you must obtain a Riverside Hall Key Access (FOB) to be able to access the labs. You can obtain a form from your department/program office. You must deliver the approved forms to the Customer Service Center in the Facilities Services Office to pick up the key.

6. All assignments and projects must be your independent work. All incidents of academic dishonesty will be dealt with according to the CSUS academic honesty, policy & procedures. The minimum sanction for each incident is that no credit will be issued to all students involved for the assignment/project. The university policy is posted at: http://www.csus.edu/umanual/student/stu-0100.htm.

7. A mailing list has been set up for the course called **csc142.** The lists will be exclusively used by the instructor to send assignments and other important information to the students. Subscription to this list is required. Follow the instructions at the following link to subscribe to the mailing list: http://hera.ecs.csus.edu/mailman/listinfo/csc142
CSc142 / CPE142 Tentative Course Outline*

<table>
<thead>
<tr>
<th>Major Topics</th>
<th>hours</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction (history &amp; Overview)</td>
<td>1</td>
<td>Chapters 1 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Instruction Set Architecture</td>
<td>1</td>
<td>Chapter 2 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Performance evaluation</td>
<td>3</td>
<td>Chapter 1 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to Computer Arithmetic</td>
<td>4</td>
<td>Chapter 3 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to Modeling in Verilog</td>
<td>4</td>
<td>Verilog HDL by Samir Palnitkar</td>
</tr>
<tr>
<td>CPU Design (Datapath &amp; control)</td>
<td>10</td>
<td>Chapters 4, and Appendix D Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Memory Design and Analysis: <em>Cache, virtual, and Interleaved memory</em></td>
<td>9</td>
<td>Chapter 5 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Interfacing and Communication</td>
<td>5</td>
<td>Patterson &amp; Hennessy</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sections 1.4, 4.9, 5.2, 5.11, 6.9, and lecture slides for the 4th edition</td>
</tr>
<tr>
<td>Parallelism</td>
<td>3</td>
<td>Chapter 6 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to distributed systems</td>
<td>3</td>
<td>Chapter 6 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Survey of contemporary architectures</td>
<td>2</td>
<td>Chapters 4, Appendix E Patterson &amp; Hennessy</td>
</tr>
</tbody>
</table>

This is just a tentative outline and does not list the topics in a chronological order. The hours listed embed three hours for exams and reviews.