1. One possible floor plan for the switched capacitor residue amp is shown below:

![Diagram of switched capacitor residue amp]

**Notes:****

1. Shields used in VREF channel and around differential inputs/outputs
2. Quiet & noisy channels on opposite sides of block to prevent noise coupling
3. Differential inputs come from & go to switches, which is why they are routed through the switch array
4. VREF's must connect to switches, so a well shielded channel must run beside the OP AMP from the quiet channel to switch array
5. Grounded wells placed under caps to reduce noise coupling from substrate
2. Focusing on the op amp portion of the floorplan from Problem #1:

- Quiet routing channel
- PMOS current sources (main)
- NMOS current sources (cascades)
- NMOS diff pairs + cascodes
- NMOS current sources (cascades)

Notes:
1) Dedicated wiring channel for VSS/VIN well shielded with VSS runs above NMOS I-sources in high metal (low C)
2) Could add VSS bus next to VDD to allow bypass caps between supplies + between VREF/VSS

Dedicated, well shielded wiring channel in high metal for op amp inputs

TO SWITCHES
TO CAPS
3. FOR THE OP AMP'S INPUT PAIR:

(a) $V = 0.35 \Rightarrow$ SMALL FETS, SO USE PLI LAYOUT AND/OR 
STEP SYMMETRY

NOTES:
1) PLI LAYOUT USED WITH 
DRAIN IN MIDDLE TO 
LOWER CAPACITANCE 

2) NMOS CASCODES ASSUMED 
ABOVE, NMOS CURRENT 
SOURCES BELOW 

3) VEE, VSN ROUTED TO 
DEDICATED CHANNEL IN 
HIGH METAL TO REDUCE C 

4) WERE TO NMOS I-SOURCE 
CAN BE IN LOW METAL 
(C & BIG PROBLEM HERE)

5) W=1, M=2, USED

(b) $V = \frac{100}{0.36} \Rightarrow$ USE SAME LAYOUT AS IN (a) FOR UNIT DEVICES, 
EXCEPT USE W=10, M=20 (TOTAL V = 10 x 20 = 200). 
ARRANGE DEVICE UNITS IN AN INTERDIGITATED 
ARRAY AS SHOWN BELOW!

\[
\begin{array}{cccccccc}
1 & 2 & 1 & 2 & 1 & 2 & 1 & 2 \\
1 & 2 & 1 & 2 & 1 & 2 & 1 & 2 \\
\end{array}
\]

NOTES:
1) COULD USE MORE UNITS AND SMALLER W, DEPENDING 
ON FREQUENCY OF OPERATION (REDUCE POLY GATE'S R)

2) COULD REVERSE ORDER OF 1, 2, 1, 2 ... IN 2ND ROW OF FETS 
TO IMPROVE CENTRING, BUT THE WIDER GATES HARDER 
AND MORE CAPACITANCE! NOTE THAT THE CURRENT LAYOUT 
ABOVE ALLOWS WERES TO PASS DIRECTLY FROM ONE DEVICE 
TO THE UNIT ABOVE IT

3) UNITS 1, 2 SHARE SOURCE DIFFUSIONS

4) CARE MUST BE TAKEN IN LAYOUT ABOVE & BELOW THIS 
DEVICE ARRAY TO MAINTAIN SYMMETRY (DUMMY ROWS 
NOT USED TO SAVE AREA)
4. For the OP AMPs NMOS current mirror:

(a) \(\frac{I_1}{I_2} = \frac{I_3}{I_4} = \frac{W_3}{W_4} = \frac{W_3}{W_4} = 0.35\), share sources, use \(W=1, M=4\) for each device \((n=2, m=2)\)

UNIT DEVICE:

DEVICE ARRAY:

(b) \(\frac{I_1}{I_2} = \frac{W_3}{W_4} = \frac{W_3}{W_4} = 0.35\) \(\Rightarrow M2\) has 10x as many units as \(M1\)! (Use same units as in \(M1\))

DEVICE ARRAY:

\[ \text{Use connected device in center of 1x centroid array} \]

\(\textbf{NOTE:} \) Arrays work best if ratios between device units are even integers, or powers of 2 (e.g., \(M2 = 4 \times M1, 8x, 16x, \text{etc.}\))