1. The switched-capacitor residue stage for a pipelined ADC is shown below. Sketch a floorplan for the layout of this block. Indicate locations for the op amp, capacitor array and switches. Also indicate how you plan to route all signals, including the differential inputs & outputs, voltage references, clocks and power supplies.

![Diagram of switched-capacitor residue stage](image)

2. The op amp used in the residue stage is shown above. Sketch a floorplan for the layout of this block. Indicate locations of all devices, as well as how you plan to route all signals and power supplies. Assume the current sources shown are PMOS cascoded.

3. Sketch a layout for the input differential pair in the op amp above if: (a) \( \beta_1 = 0.35 \), (b) \( \beta_2 = 200 \), 0.35. Be sure your layout achieves good matching. Show all metal hook-up in your sketch.

4. Sketch a layout for the NMOS current mirror shown in the op amp above if: (a) \( \beta_1 = \beta_2 = 0.35 \), (b) \( \beta_1 = \beta_2 = 0.25 \). Be sure to work for good matching and show all metal hook-up.