Sample and Hold (S/H)

- Basic function of this block is to sample a continuous time signal and hold the result.
- "Track and Hold" blocks are similar, but in these the output tracks the input part of the time.

\[ \text{OR,} \]

\[ \text{OR, CAN ALSO BE:} \]

- S/H with "return to zero" on Vout during sample phase.
- S/H circuits often used prior to ADCs.
  - Eliminates errors due to timing differences by "pre-sampling" the data before the ADC.
Sample and Hold Performance Parameters (specs)

1. "Sampling Pedestal" or "Hold Step"
   - Occurs every time S/H enters hold mode (e.g., charge injection from switch turn off)
   - If this is "signal dependant", can cause distortion! ➔ make signal independent for good linearity!

2. Input Bandwidth
   - -3dB frequency limits how fast the S/H can follow high frequency input signals
   - May also be limited by slew rate

3. "Aperture Jitter" or "Aperture Uncertainty"
   - Variation of sampling times from ideal
   - Causes errors in sampled voltage
   - Error increases as input frequency goes up

4. "Droop Rate"
   - Slow change in held voltage, due to PN junction leakage currents (typically)
   - Less important for S/H operating at high freq

5. "Hold-mode Feedthrough"
   - Measure of how much Vin couples to Vout during hold mode (ideally = 0)
   - Typically due to parasitic capacitors (e.g., Cps)

Other specs: gain error, offset error, linearity, dynamic range
Simple Sample and Hold

- CMOS technology provides good switches + caps!

- Open loop track & hold (no feedback to reduce errors)
- Passive sample (just looks like R-C)

1) Sample phase: When CLK = high, the MOS switch is on, causing Vout = V = Vin

2) Hold phase: When CLK goes low, the MOS switch turns off, storing the value of Vin on C

Charge-injection errors

- When M1 turns off, it "injects charge" onto C causing the stored voltage to have an error

→ "Channel charge" = charge stored in channel of "on" FET which dumps onto C when FET turns off

→ "Clock feed-through" = charge coupled onto storage cap from clock, through C65
CHARGE INJECTION ERRORS (CONT.)

\[ Q_{CH} = (V_{GS} - V_T) C_{GATE} = (V_{DD} - V_{IN} - V_T)(WLCOX) \]

ASSUME \( \frac{1}{2} Q_{CH} \) FLOWS ONTO \( C^* \) \( \Rightarrow \) \( * \) True for fast clk edges

\[ \Delta V_1 = \frac{1}{2} \frac{(WLCOX)}{C} (V_{DD} - V_{IN} - V_T) \]

AND, \( \Delta V_1 \) IS “SIGNAL DEPENDANT” \( \Rightarrow \) DISTORTION!

ERROR DUE TO CLOCK FEED-THROUGH!

* CLOCK IS COUPLED ONTO \( C \) THROUGH \( C_{OV} = \) OVERLAP CAP, AFTER MOS SWITCH TURNS OFF \( \Rightarrow \)

\[ \Delta V_2 = \frac{(WL_{OV}COX)}{C} (V_{IN} + V_T) \]

(ASSUMES FET TURNS OFF WHEN \( VOL = V_{IN} + V_T \))

\( \Delta V_2 \) ALSO SIGNAL DEPENDANT.

TOTAL = \( \Delta V_1 + \Delta V_2 \)

NOTES:
1. RESULTS ABOVE ARE SLIGHTLY DIFFERENT THAN IN TEXT:
   a) TEXT ASSUMES CLOCK GOES FROM \( V_{DD} \) TO \( V_{SS} \) (E.G., \( \pm 2.5V \)), WHICH CAUSES THE CHANNEL CHARGE ERROR DUE TO \( V_{IN} \) TO APPEAR AS A LINEAR GAIN ERROR (\( V_T \) ERROR STILL NONLINEAR)
   b) TEXT COUNTS CLOCK FEED-THROUGH EVEN WHEN SWITCH IS ON! (EITHER NOT TRUE, OR \( C \neq C_{OV} \) WHEN FET IS ON!)

2. CHANNEL CHARGE ERRORS ARE USUALLY \( >> \) CLOCK FEED-THROUGH
EXAMPLE 8.1

Consider the sample and hold of Fig. 8.3 with $C_{hh} = 1 \text{ pF}$, $C_{ox} = 1.92 \text{ ff/}(\mu\text{m})^2$, $V_{in} = 0.8 \text{ V}$, and $(W/L)_r = (5 \text{ mm}/0.8 \text{ mm})$. Assume the power supply voltages are $\pm 2.5 \text{ V}$ and the input signal is $1 \text{ V}$ peak to peak. Find the hold step for $V_{in}$ equal to $1 \text{ V}$, and then repeat for $V_{in}$ equal to $-1 \text{ V}$. Use the estimates for errors at $\pm 1 \text{ V}$ to estimate the dc offset.

Solution

At $V_{in} = 1 \text{ V}$, using (8.3), we find $AV'(1 \text{ V}) = -2.69 \text{ mV}$. At $V_{in} = -1 \text{ V}$, again using (8.3), we find $AV'(-1 \text{ V}) = +10.36 \text{ mV}$. The average offset is given by

$$V_{offset-avg} = \frac{AV'(1 \text{ V}) + AV'(-1 \text{ V})}{2} = \frac{-2.69 \text{ mV} + 10.36 \text{ mV}}{2} = 6.53 \text{ mV}$$

which is a reasonable estimate of the amount of dc offset injected in this example.

![Diagram of an op-amp circuit](image)

Fig. 8.3  An open-loop track and hold realized using MOS technology.

**ANOTHER WAY TO LOOK AT IT!**

**NOT INCLUDING $V_{in}$**

$\Rightarrow AV = -\frac{C_{ox}WL(V_{DD} - V_{in})}{2C_{hh}} = -6.53 \text{ mV}$

**LOOKS LIKE AN OFFSET!**

**DUE TO $V_{in}$**

$\Rightarrow AV = -\frac{C_{ox}WL(-V_{in})}{2C_{hh}}$

**EQUAL ERRORS FOR $\pm V_{in}$**

For: $V_{in} = +1 \Rightarrow AV = +3.84 \text{ mV}$

$V_{in} = -1 \Rightarrow AV = -3.84 \text{ mV}$

**LOOKS LIKE A GAIN ERROR!**

**TOTAL ERROR**: $V_{in} = +1 \Rightarrow -6.53 + 3.84 = -2.69 \text{ mV}$ **SAME AS**

$V_{in} = -1 \Rightarrow -6.53 - 3.84 = -10.37 \text{ mV}$ **ABOVE!**

**NOTE**: **IF $V_{in}$ (COMMON-MODE) $\neq 0$** $\Rightarrow$ **ADDITIONAL $V_{os}$ TERM!**
**Possible Ways to Cancel Charge Injection**

- If PMOS & NMOS switches are made the same size, then this will cancel charge injection somewhat... but,
  \[ Q_{PMOS} \neq Q_{NMOS} \] as \( V_{IN} \) varies!
  \( \Rightarrow \) **not typically used to cancel charge injection**!
  (CMOS T-gate at input is used to pass \( V_{IN} \) over large voltage range)

- "dummy" switch added to cap side of main switch
  \( \rightarrow \) Make it \( \frac{1}{2} \) size of main switch to dump \( \frac{1}{2} \) charge
  \( \rightarrow \) Clock it with \( CLK \)
  \( \Rightarrow \) Works OK, to the extent the FETs can be matched
  \( \sim 20 \text{dB} \) reduction can be achieved.

**Best Ways to Reduce Charge Injection Errors**:

1) **Make switches as small as possible!** (\( Q = \text{small} \))

2) **Make \( Q \) injected non-signal dependent!**
   \[ \rightarrow \text{Signal dependent } Q \text{-injection } \Rightarrow \text{Distortion!} \]
   \( \text{Bad!} \)
   \[ \rightarrow \text{Non-signal dependent } \Rightarrow \text{offsets} \]
   \( \text{(doesn't hurt linearity)} \)
**Sampling Jitter**  (due to finite clock edges)

![Diagram of sampling jitter](image)

Fig. 8.6 The clock waveforms for $V_{in}$ and $\phi_{clk}$ used to illustrate how a finite slope for the sampling clock introduces sampling-time jitter.

- **Assume the ideal sample times are when the falling edge of clk passes through V**

- **The actual sample times vary with Vin, since the n-fet turns off when $V_{on} = V_{in} + V_t$**

  \[ \Rightarrow \text{signal-dependent errors!} \Rightarrow \text{distortion!} \]

**Example 8.2**

Consider the S/H circuit of Fig. 8.3, where $V_{in}$ is a 20-MHz band-limited signal with a 2-V peak amplitude. Assume that $\phi_{clk}$ is a 100-MHz square wave having a peak amplitude of ±2.5 V with linear rise and fall times of 1.5 ns. What is the maximum uncertainty of the sampling time? Assume $V_{in}$ is 0.8 V.

**Solution**

First, we note that the slope of $\phi_{clk}$ is $(5 \text{ V}) / (1.5 \text{ ns}) = 3.33 \text{ V/ns}$, and the true sampling time is when the clock waveform is 0.8 V greater than the input signal.

For $V_{in}$ equal to 1 V, the sampling transistor will turn off when $\phi_{clk}$ is 1.8 V, which is $(0.7 \text{ V}) / (3.33 \text{ V/ns}) = 0.21 \text{ ns}$ after the clock first starts to move down.

When $V_{in}$ is $-1$ V, the sampling time occurs when $\phi_{clk}$ is $-0.2$ V, which is $0.81$ ns after the clock first starts to move upward.

Therefore, the sampling-time uncertainty is $0.81 - 0.21 = 0.6$ ns. Also, assuming the ideal sampling time is $0.75$ ns after the clock first starts to move, the sampling jitter is from $-0.54$ ns to $+0.06$ ns from the ideal sampling time.
**Sampling Jitter (cont.)**

- **Even if clock edges were perfectly sharp (step function), all real clocks have jitter!**

  "**Jitter**" = variation in time when clock edges occur as compared to ideal edge time.

  \[ \Delta t \]

  - **Jitter Numbers:** Can vary from a few psec peak-to-peak, to a few nsec. What is considered "good" depends on your application!

---

**Example:** If a clock with 100 psec peak jitter and perfectly sharp edges is used to sample an input sine wave at 10 MHz with amplitude = 1 V, what is the max error?

**Solution:** The maximum error will occur as the input sine wave is sampled at \( V_{in} = 0 \), since this is where \( V_{in} \) has the max slope.

\[
V_{in}(t) = A \sin(wt) \]

\[
\frac{\Delta V}{\Delta t} = A w \cos(wt) \]

\[ \Rightarrow \text{Max} = A w \text{ slope} \]

\[ V_{error} = \Delta \text{error} \times \text{slope} \]

\[
A = 1 \]

\[
w = 2\pi \text{ (10 MHz)} \]

\[
\Rightarrow \max \text{ slope} = 6.28 \times 10^7 \text{ V/s} \]

\[
\Rightarrow \max \text{ error} = (0.1 \text{ ns}) \left( \frac{6.28 \text{ mV}}{\text{ns}} \right) = 6.28 \text{ mV} \]

\[ \text{Max error} = 6.28 \text{ mV} \]

*Note that this would go up to 62.8 mV for a 100 MHz sine wave, independent of the clock frequency.*


**ALTERNATE S/H CIRCUITS**

![Diagram](image)

**Fig. 8.7** Including an opamp in a feedback loop of a sample and hold to increase the input impedance.

- **Input of amp increases input resistance, and reduces Vos (offset) due to output buffer**

  **But, when clk = 0 ⇒ no feedback! ⇒ Vout of amp 1 rails at Vdd or GND! (bad!)**

  **(Must recover on next sample!)**

  **→ slow!**

![Diagram](image)

**Fig. 8.8** Adding an additional switch to the S/H of Fig. 8.7 to minimize slewing time.

- **Adding switches Q2, Q3 keeps amp1's output from slewing to the rail**

  **→ same as previous clk when clock = high**

  **→ amp1 is in unity gain feedback when clock = low (after sample)**

  **⇒ amp1 does not have to slew from Vdd or GND on every sample! Instead, it's output voltage is already ≈ vin. ⇒ much faster!**
**Alternate S/H Circuits (Cont.)**

Fig. 8.9 An improved configuration for an S/H as compared to that of Fig. 8.8.

- **Since Op Amp 2 forces a "Virtual Ground" at its - input \(\Rightarrow\) charge injection due to \(Q_1\) is \text{signal-independent!}\)
  \(\Rightarrow\) offset, but no distortion!

- **But, now Op Amp 2 must be a \text{high gain} Op Amp, and, the \text{bandwidth} of Op Amp 2 affects the sample time \(\Rightarrow\) "active sampling".

- \(Q_2\) used to keep the output of Op Amp 1 from railing.

Fig. 8.10 An S/H similar to that of Fig. 8.9, but with clock-feedthrough cancellation circuitry added.

- **Build a circuit on the + input of Op Amp 2 to "mimic" the charge injection on the - input \(\Rightarrow\) makes error voltage look like a common-mode input \(\Rightarrow\) reduces "effective" offset voltage, \(V_{os}\)

"**Quasi-Differential**" circuits can reduce errors by \(\approx 20\)dB max.
**ALTERNATE S/H CIRCUITS (CONT.)** (MANY MORE EXIST!) (SEE TEXT FOR MORE)

![Diagram of a simple switched-capacitor S/H circuit]

- **DURING $\phi_1$:** $V_{IN}$ IS STORED ON $C_H$ \[ V_{CH} = V_{IN} - V_{OS} \]
  - $V_{OS}$ IS STORED ON $C_H$

- **DURING $\phi_2$:** $C_H$ IS PUT INTO FEEDBACK AROUND THE OP AMP $\Rightarrow$ $V_{OUT} = V_{IN}$ (VOS IS CANCELLED)

**BUT, DURING THE SAMPLE PHASE THE OP AMP MUST SETTLE $\Rightarrow$ REQUIRES A FAST OP AMP!**

(AND WHAT IF $V_{IN}$ IS MOVING?)

**A BETTER WAY:**

- **PASSIVE SAMPLE** (OP AMP DOESN'T NEED TO SETTLE)
- **DOESN'T CANCEL $V_{OS}$**
- **CAN MAKE CHARGE INJECTION SIGNAL INDEPENDENT EASILY**

(MORE ON THIS LATER...)
FULLY DIFFERENTIAL S/H

\[ V_{IN} = V_{IP} - V_{IN} \]
\[ V_{OUT} = V_{OP} - V_{ON} \]

**Advantages:**
1. **Noise appears common-mode** (E.g., noise on VDD)
2. **Charge injection due to M1, M2 appears as common-mode** → no Vos if M1 matches M2!
3. **Charge injection due to T-gates can be eliminated easily** (more on this later...)
4. **Passive sampling** → no op amp to settle during sample
5. **Fast!** Charge stored on C during sample stays on C during hold; good feedback factor (more later...)

**Dis-advantages:**
1. Requires 2 of everything but op amp (caps, switches)
2. Requires differential op amp (bigger, needs common-mode feedback)

"Virtually all mixed-signal circuits today are fully differential!"