Transistor Level Opamp Design

- Gains for amps range from 20-100 dB and sometimes even higher

- Opamps employed in F.B.
  
  ° AoL chosen based on required system precision
  
  \[
  A_f = \frac{A_{OL}}{1 + \beta A_{OL}}
  \]

  ° Opamps no longer "general purpose" but more application specific

- Many parameters to trade-off

**Example**

Assume a gain of 10 is required

\[1 + \frac{R_2}{R_2} = 10\]

\[A_{OL} = ?\] for 1% gain error

Recall \(A_f\) & derivation of closed loop gain

\[
\frac{V_o}{V_i} = \frac{A_{OL}}{1 + \frac{R_2}{R_1 + R_2} A_{OL}}
\]

° 1% is a small gain error \:. Large \(A_{OL}\) will be required to get 1% error

\[9.99 = \frac{A_{OL}}{1 + 0.1(A_{OL})}\]

\[\Rightarrow A_{OL} \approx 10,000 \text{ or } 80 \text{ dB}\]

- Attempting a gain of 10 by using a CSA stage with an error = 1% is quite difficult

\[
\frac{V_o}{V_i} = -g_m R_D \quad \text{but } R_D \text{ varies by } \pm 30\%
\]

\[g_m = \frac{1}{2} \mu n C_o x \frac{W}{L} (V_{gs} - V_T)\]

\[\text{\& varies due to process \& temp.}
\]

\[\text{Process, geometry}\]
Small signal Bandwidth

frequency behavior

Note that $A_{ol}$ decreases with frequency
hence: $A_f = \frac{A_{ol}}{1 + \beta A_{ol}}$ has larger error

Example

$V_i \rightarrow V_{in}$ step function, small signal
$\tau = ?$ for output voltage to reach 1% of final value

$$\frac{V_o}{V_i} = \frac{A_{ol}(cs)}{1 + \frac{R_1}{R_1+R_2} A_{ol}(cs)}$$
$$\frac{R_1}{R_1+R_2} = \beta$$

Assume opamp exhibits 1 pole behavior, then:

$$A_{ol}(cs) = \frac{A_{ol}}{1 + \frac{s}{\omega_0}}$$

$$\frac{V_o(cs)}{V_i(cs)} = \frac{A_{ol}}{1 + \frac{s}{\omega_0} + \beta A_{ol}}$$
place in standard form

$$A(cs) = \frac{K}{1 + \frac{s}{\omega_0}}$$

$$= \frac{A_{ol}}{1 + \beta A_{ol}}$$

$$= \frac{s}{1 + (1+\beta A_{ol}) \omega_0}$$

The closed loop amplifier will show as a 1 pole ckt with $\tau = \frac{1}{(1+\beta A_{ol}) \omega_0}$
Assume $V_i(t) = a u(c t)$ then $V_i(s) = \frac{a}{s}$

$$V_0(s) = \frac{\frac{A_{ol}}{1 + \beta A_{ol}}(\frac{a}{s})}{1 + \frac{s}{(1 + \beta A_{ol})w_0}}$$

$$V_0(s) = \frac{aA_{ol}w_0}{s((1 + \beta A_{ol})w_0 + s)}$$

Use partial fraction expansion

$$\frac{aA_{ol}w_0}{s((1 + \beta A_{ol})w_0 + s)} = \frac{B_1}{s} + \frac{B_2}{(1 + \beta A_{ol})w_0 + s}$$

$$B_1 [(1 + \beta A_{ol})w_0 + s] + B_2 s = aA_{ol}w_0$$

$$B_1 (1 + \beta A_{ol})w_0 = aA_{ol}w_0 \implies B_1 = \frac{a}{\beta}$$

$$B_2 = -\frac{a}{\beta}$$

$$V_0(s) = \frac{\frac{a}{s}}{s + \frac{\beta A_{ol}w_0}{s}} \implies V_0(t) = \frac{a}{s^2} \left[ 1 - e^{-\frac{t}{\tau}} \right]$$

$$\tau = \frac{1}{\beta A_{ol}w_0}$$ for $\beta A_{ol} \gg 1$
So \( v_0(t) = \frac{a}{v}\left[1 - e^{-t/\tau}\right] \). \( t \to \infty \) \( v_0 \to \frac{a}{v} \frac{4}{\tau} = a\left(1 + \frac{R_2}{R_1}\right) \).

For 1% settling time

\[ v_0(t) = 0.99 \, v_0f \]

\[ \frac{a}{v} \left[1 - e^{-t/\tau}\right] = 0.99 \frac{a}{v} \text{ or } \left[1 - e^{-t/\tau}\right] = 0.99 \]

Solve for \( t \) \( \implies t_S = 4.6 \, \tau \).

b) Assume need \( A_0 \approx 10 \) & a 5ns settling time. Further assume that \( A_{cs} \left|_{\text{low frequency}} \right. \gg 1 \). What \( \text{UGB} \) must op-amp provide?

\( t_S = 5 \text{ns} \implies 5\text{ns} / 4.6 = 2 \implies \tau \approx 1.09 \text{ns} \)

but \( \tau \approx \left(1 + \frac{R_2}{R_1}\right) \frac{1}{A_{ol} \omega_0} \text{ or } \frac{1}{\beta A_{ol} \omega_0} \)

\[ \omega_0 = A_{ol} \omega_0 = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{\tau} = 9.21 \text{ Grad/s} \text{ or } 1.47 \text{ GHz} \]

Opamps require (wish list):

- Large Bandwidth
- Output Swing
- Linearity
- Noise & offset tolerance
- Supply rejection
One stage Amps

\[ A_{V} = g_{m1} \left( \frac{r_{o2}}{r_{in}} \right) \]

use s.e. amp as buffer

\[ A_{f} = \frac{A_{oL}}{1 + \beta A_{oL}} \]

note voltage F.B. used at output \( \Rightarrow \) output resistance in open loop divided by \( (1 + g_{m} (r_{on}/r_{op}) ) \) is the output resistance

\[ R_{out} = \frac{r_{on} \parallel r_{op}}{1 + g_{m} (r_{on} \parallel r_{op})} \approx \frac{1}{g_{m}} \]
High Gain topologies

node \rightarrow current mirror is also cascode for high gain

\text{Gain} = g_{mn} \left[ (g_{mn} r_{on}^2 \# g_{mp} r_{op}^2) \right]

for \( g_{mn} r_{on}^2 = g_{mp} r_{op}^2 \)

\text{Gain} \approx g_{mn} \left( g_m \frac{r_o^2}{2} \right) \approx g_m \frac{r_o^2}{2}

overall swing limited

\begin{align*}
\text{VDD} & \quad \{ \text{Hashed area is min. requ. by bias} \\
\text{VDD - 2}\Delta V & \text{V}_{\text{in}} \} \\
\text{VSS + 3}\Delta V & \text{gnd}
\end{align*}

Difficult to short terminal & output (use as buffer)

\text{Must keep H2 & H4 saturated}

\begin{align*}
\text{V}_0 & \leq \text{V}_x + \text{V}_{\text{t}2} \quad \text{to keep H2 alive} \\
\text{V}_0 & \geq \text{V}_b - \text{V}_{\text{t}4} \quad \text{to keep H4 alive}
\end{align*}

\therefore \quad \text{V}_b - \text{V}_{\text{t}4} \leq \text{V}_0 \leq \text{V}_x + \text{V}_{\text{t}2}

\text{but } \text{V}_x = \text{V}_b - \text{V}_{\text{gs}4}

\therefore \quad \text{V}_b - \text{V}_{\text{t}4} \leq \text{V}_0 \leq \text{V}_b - \text{V}_{\text{gs}4} - \text{V}_{\text{t}2}
Graphically

\[ V_b \]

\[ V_b - V_{t4} \leq V_0 \leq V_b - V_{gs4} + V_{t2} \]

useable range limited!

- Opamp performance at these biasing conditions
  - Opamp will force \( V_o = V_i \)
  - \( V_i < V_b - V_{t4} \) \( V_o \approx V_i \) & \( M4 \) is in triode & other xtrs saturated
  - Result \( \Rightarrow \) Reduction of open loop gain
  - For \( V_i \) in between \( V_o \approx V_i \) & all xtrs sat & gain maxed out
  - For \( V_i > V_b - V_{gs4} + V_{t2} \) \( M2 \) & \( M1 \) \( \Rightarrow \) triode degrading gain

Design Example

Design fully differential cascode amp \( V_{dd} = 3V \), \( V_{dd} = 3V \), Power = 10mW

\[ A_{ol} = 2000 \] \( \mu nC_{ox} = 60 \mu A/V^2 \)

\[ \mu pC_{ox} = 30 \mu A/V^2 \]

\( M_{b1} \) & \( M_{b2} \) define currents for

\[ \lambda_n = 0.1 V^{-1} \] \( \lambda_p = 0.2 V^{-1} \)

\[ V_{en} = |V_{bp}| = 0.7 \]

\( \lambda \) for \( L = 0.5 \)

Available current \( P = I \times V \)

\[ I = \frac{10mW}{3V} = 3.33 \text{ mA} \]
Provide 3mA to H9 & 330μA between Hb1 & Hb2

each codec branch carries 1.5mA

nodes x & y must swing 1.5V w/o causing H3-H6
to operate in triode

If 1.5V used up in swing then 3-1.5 = 1.5 remains for
biasing

ΔV₁ + ΔV₅ + ΔV₃ + ΔV₁ + ΔV₉ = 1.5

H9 carries largest current provide 0.5V = ΔV₉

M₅,6,7,8 are P channels & have low mobility provide 0.3V = ΔV₅/₆,7,8

H₁,2,3,4 have ΔV₁₂₃₄ = 0.2

\[ I_D = \frac{1}{2} \mu \tau C_0 W^2 \left( \frac{V}{L} \right)^2 \]

\[ (\frac{W}{L})_{1-4} = 1.25 \]

\[ (\frac{W}{L})_{5-8} = 1.11 \]

\[ (\frac{W}{L})_9 = 400 \]

\[ R_0 = \frac{1}{\lambda I_D} \]

\[ A_V \approx g_{m1} \left( \frac{g_{m3} R_{03} R_{01}}{(g_{m5} R_{05} R_{07})} \right) \]

\[ R_{0_{1,3}} = \frac{1}{0.1 \text{ (1.5mA)}} = 6.7 \text{ kΩ} \]

\[ R_{0_{5,7}} = \frac{1}{0.2 \text{ (1.5mA)}} = 3.3 \text{ kΩ} \]

\[ g_m8R = \frac{2I_D}{0.3} = 10 \text{ mA/V} \]

\[ g_{m13} = \frac{2I_D}{0.2} = 15 \text{ mA/V} \]

\[ A_V \approx 15 \text{ mA/V} \left[ \frac{(15)(6.7k)(6.7k)}{(10)(3.3k)(3.3k)} \right] \]

≈ 15 mA/V \left[ \frac{(673.33k)}{(1089k)} \right] = 15 \text{ mA/V} \left( \frac{93.7}{400} \right) = 14.06 \]

not enough gain! must increase channel length but on which devices?
H1,2,3,4 are on signal path keep their \( L \) minimum to keep capacitances to a minimum.

H5,6,7,8 are good candidates, not directly in signal path.

Double \( L \) \( \Rightarrow \) double \( g_{mR_0} \) \( \Rightarrow \) \( g_m \) remains the same.

\( R_0 \) doubles \( \Rightarrow \) \( g_{mR_0} \) doubles.

\[
\text{make } (w/L)_{5-8} = 2222/1.0 \quad \text{&} \quad \lambda p = 0.1V^{-1} \quad \lambda \propto \frac{1}{L}
\]

New gain \( A_u \approx 4000 \) or 72 dB \( \Rightarrow \) can shrink length \( \Rightarrow \) width & size of MOS since \( 1/2 \) that gain is required.

Minimum allowed \( V_{CH} = V_{GS1} + \Delta V_q = 1.4V \)

Minimum allowed \( V_{b1} = V_{GS3} + \Delta V_1 + \Delta V_q = 1.6V \)

Maximum allowed \( V_{b2} = V_{DD} - (1V_{GS1} + 1\Delta V_1) \)

\[
= 1.7V
\]

- \( V_{b1}, V_{b2} \) must be given margin to account for process & other variations.
- Did not include body effect.

Telescopic Amp \( \Rightarrow \) limited output swing.

Must exercise caution when shorting input & output.

Use "folded cascode" to improve circuit performance.

Telescopic cascades remain very useful building blocks for design.
Problem with cascodes (telescopic) is device "stacking" that occurs → folded cascode removes part of issue

"telescopic"

"folded"

Consumes more current
telescopic $\rightarrow V_{in,colm} < V_{b1} - V_{gs3} - V_{b1}$

folded $\rightarrow V_{in,colm} > V_{b1} - V_{gs3} - V_{b1p1}$
much easier to short output & input

assuming $V_{b1} & V_{b2}$ provide adequate bias

swing @ bottom

$\Delta V_{S} + \Delta V_{S}$

swing on top

$V_{DD} - \Delta V_{T} - \Delta V_{Q}$

- Note that M5 & M6 carry substantial current

- Must make overdrive of M5 & M6 large to balance capacitance @ node X & Y

$\frac{I_D}{W/L} = \frac{V_{gs} - V_{T}}{L} C_{ox}$

make larger $W/L$

shrinks $W/L$

lowers capacitance

short ckt transconductance (small signal)

Host of current goes through M3

$\frac{1}{(g_{m3} + g_{mbs})} \parallel \frac{1}{R_{O3}}$

$\frac{R_{O5}}{\parallel R_{O1}} \rightarrow \frac{1}{g_{m} \approx g_{m1}}$
\[ R_{op} \approx (g_{m7} + g_{mb7}) R_7 R_{q9} \]

\[ R_{out} = R_{op} // [ (g_{m3} + g_{mb3}) R_3 (R_{10} || R_{50}) ] \]

but \( A_{in} = g_m R_{out} \)

\[ \therefore A_{in} \approx g_m [ (g_{m3} + g_{mb3}) R_3 (R_{10} || R_{50}) // (g_{m7} + g_{mb7}) R_7 R_{q9} ] \]

- PMOS differential input has lower transconductance
- \( R_{10} \) and \( R_{50} \) are in parallel reducing \( R_{out} \)
- Gain for folded cascode about 2 to 3 times lower than equivalent telescopic cascode configuration

\[ \begin{align*}
V_{b1} & \quad [3] \\
V_i & \quad [1] \\
C_{total} & \quad [C_{g3} + C_{sb3} + C_{d1} + C_{gd1}]
\end{align*} \]

note source of \( H_3 \) higher in potential for this config. Significant body effect

\[ c_{total} \text{ contributed to by:} \]

\[ c_{gs3} + c_{sb3} + c_{d1} + c_{gd1} \]

\[ \text{telescopic cascode} \]

\[ \text{Cddbs} \text{ and } C_{gds} \text{ can be large since } H_5 \text{ usually has to sink large currents with small } \Delta V \therefore \text{large size} \]
- Potentially higher gains with this circuit because of better $g_m$.
- Cost is bandwidth reduction.
  Pole at node $X$ given by $\left[ R_0 \parallel \left( \frac{1}{g_{m3} + g_{mb3}} \right) \parallel R_0 \right]^{-1} \left[ c_{ef} \right]^{-1}$.
  $\approx \frac{g_{m3}}{c_{ef}}$.
- P channel devices are larger than n-channel devices due to lower hole mobility $\rightarrow$ loose on $c_{ef}$.
- P channels have lower $g_m \therefore$ loose on $g_{m3}$.
- Folded cascode costs higher power, has lower gain, lower pole frequency but can be easily used as buffer, CH easier to deal with, & better swing.
$V_{DD} = 3\, V$, output swing $3\, V$, Power dissipation 10mW (N-input)

- Allow 1.5mA for input pair, 1.5mA to cascode branches & remainder 330mA to current mirrors

- M5 & M6 carry 1.5mA: make $\Delta V$ large to keep size small

$\Delta V_{5/6} = 500\, mV \quad M_{5/4} \rightarrow \Delta V = 400\, mV \quad M_{7-10} \rightarrow \Delta V = 300\, mV$

$(W/L)_{5/6} = 400 \quad (W/L)_{3/4} = 313 \quad (W/L)_{7-10} = 655$

for $\mu_n C_{ox} = 60\, \mu A/V^2 \quad \mu_p C_{ox} = 30\, \mu A/V^2 \quad \lambda_n = 0.1\, V^{-1} \quad \lambda_p = 0.2\, V^{-1}$

$V_{TN}, V_{TP} = 10.7 \quad \gamma = 0$

\[\begin{align*}
\Delta V_5 &= 400\, mV \rightarrow 300\, mV \rightarrow 500\, mV \\
\therefore \quad 3V - 0.4\, V - 0.5\, V &= 2.1\, V \\
0 + 0.3 + 0.3 &= 0.6 \\
\therefore \quad \text{CM} &\rightarrow 1.35\, V \quad \text{for output} \\
M_{min} \, \text{CM} &= \Delta V_1 + \Delta V_{iss} \\
\Delta V_{1,2} &= 0.2\, \mu A \quad (W/L)_{1,2} = 400
\end{align*}\]

Dimensions of M1 & M2 determined by input capacitance requirements & output cap.

$g_m = \frac{2I_D}{\Delta V}$

$g_{m1,2} = 6\, mA/V \quad g_{m3,4} = 0.0038\, mA/V \quad g_{m7,8} = 50\, mA/V$

$L = 0.5\, \mu m \quad R_{1,2,7,10} = 13.3k\Omega \quad R_{3,4} = 2R_{5,6} = 6.67\, k\Omega$

\[\begin{align*}
\therefore \quad \text{looking into drain M7, M8 resistance is } 88\, k\Omega \\
\text{looking into } M3, M4 \quad \therefore \quad 66.5k\Omega
\end{align*}\]

\[\begin{align*}
\therefore \quad \text{gain } \times 400
\end{align*}\]
Current Mirror Opamp

Basic topology

- Nodes 1, 2, 3 are "low impedance" so they give rise to low gain.
- Node 4 is the only high impedance node.
- With simple current mirrors gains of 40dB & below are achievable.
- Higher gains require cascode current mirrors.
- Note that the current is scaled from the input stage to the output stage.

\[
g_m = \frac{2ID}{V_{gs} - V_t} \quad \therefore \text{for the same } \Delta V \text{ more current gives higher } g_m \& \text{ in our case the factor is } K
\]

- The gain at the output is

\[
R_{out} = \frac{R_6}{R_8} \\
g_{mout} = Kg_{m1} \\
\therefore \text{gain @ low frequencies is} \quad \text{Gain} = Kg_{m1}R_{out}
\]
- The output pole is based on the $\frac{1}{\text{RoT}^2 C_L}$ product.
- Assuming good separation between dominant & non-dominant poles

\[ A_v = \frac{K_{\text{gm}1}\text{RoT}}{SC_{\text{RoT}^2} + 1} \]

- Note as $s \to 0$ the gain is $K_{\text{gm}1}\text{RoT}$
- For high frequencies the "1" term in the denominator is swamped out

\[ A_v \approx \frac{K_{\text{gm}1}\text{RoT}}{SC_{\text{RoT}^2}} = \frac{K_{\text{gm}1}}{SC_L} \]

- The unity gain frequency requires $A_v = 1$.

\[ \omega_{u.g.} = \frac{K_{\text{gm}1}}{C_L} = \frac{K \sqrt{2 I_{D1} / n \text{Cox}(\omega C_L)}}{C_L} \]

- Note that the higher the $K$ factor, the higher the gain.
- The current mirror gain $K$ cannot be increased indefinitely.
  - Internal nodes contribute to time constants also.
  - With large (greater-than 4Ωs) $K$ factors it may not be possible to have well separated poles while achieving useful bandwidth.
  - Typical $K$ factors are between 2 to 5.

- Note that in the "generic" circuit node 1, 2, & 3 give rise to non-dominant poles.
- Increasing $K$ increases the capacitances at nodes 1, 2, & 3 & the resistances at the reference side of the current mirror.
- Current on input side is smaller and so are the widths.
- As a result the $g_m$ is smaller on the input side and $V_{g_m}$ results in a higher resistance.
- This causes the non-dominant poles to move closer to the dominant one.
- Increasing $K$ also increases the capacitance on the non-dominant nodes making the overall impedance larger.
- In order to maintain stability $C_L$ may need to grow.
- So $K$ cannot be made arbitrarily large.
- Good rule is 1 to 2 for a $K$ factor for small $C_L$ when bandwidth is key.
- Slew rate causes the tail current to be diverted through either N1 or H2 & multiplied by $K$ on its way to the output.
- The total current available to charge $C_L$ is $K I_{bias}$

$$SR = \frac{K I_{bias}}{C_L}$$

- High gain realization with wide-swing cascodes.
- Bias networks can be combined more effectively but not shown in this diagram that way.