California State University, Sacramento
CpE 151 – Spring 2007

**Project 2**

**Design and Layout of a Bubble Suppress and Decode Logic circuit for a 3-bit Flash ADC**

**DESIGN OVERVIEW:**

This project is to design and layout a bubble suppress and decode logic circuit for a 3-bit Flash analog-to-digital converter (ADC). A simplified schematic of this ADC is shown below, both with and without a bubble in the thermometer code to illustrate the concept of bubbles. Note that the values of the bits shown in the thermometer and output codes in the figure are just examples. All bits can be either a 0 or 1, depending on the value of the input voltage. Your design should give the correct output code even if a bubble is present. (Hint: Your bubble suppress circuit should use 3 comparator outputs to decide where the transition is between 0’s and 1’s in the thermometer code, not just a single comparator output.) Also, the final ADC output code should be stored in 3 flip-flops and then connected to output pads, which are not shown in the figure.

![Diagram of 3-bit Flash ADC with and without bubbles](image-url)
DESIGN SPECIFICATIONS:

- Design each logic gate for its transient performance. The rise time and fall time should be equal. Adjust the aspect ratios appropriately, but do not use the Elmore formula.
- Technical specifications:
  - Mobility of electrons: $\mu_n = 600 \text{ cm}^2/\text{V-sec}$
  - Mobility of holes: $\mu_p = 200 \text{ cm}^2/\text{V-sec}$
  - Oxide thickness: $t_{ox} = 110 \text{ Å}$
  - Threshold voltage for p type: $V_{tp} = -0.60 \text{ V}$
  - Threshold voltage for n type: $V_{tn} = 0.60 \text{ V}$
  - Channel length: $L = 2 \mu\text{m}$
  - Channel overlap distance: $L_o = 0.2 \mu\text{m}$
  - Junction depth: $x_j = 3 \mu\text{m}$
  - Load capacitance: $C_L = 150 \text{ fF}$ (Load for output bits B[3:0] and overflow)
  - N diffusion junction capacitance: $C_{jn} = 0.35 \text{ fF}/\mu\text{m}^2$
  - P diffusion junction capacitance: $C_{jp} = 0.45 \text{ fF}/\mu\text{m}^2$
  - N diffusion sidewall capacitance: $C_{jswn} = 0.40 \text{ fF}/\mu\text{m}$
  - P diffusion sidewall capacitance: $C_{jswp} = 0.40 \text{ fF}/\mu\text{m}$
  - Supply voltage: $V_{dd} = 3 \text{ V}$
- Calculate the mid voltage, rise time and fall time of every logic gate.
- Consider one unit ($\lambda$, one grid) equal to 1 $\mu\text{m}$.
- Area used should be as small as possible (minimize unnecessary “white space”).

Phase - I: Design Work (Due: April 24th, 2007, at the beginning of class)

In this phase, students will design the circuit and also calculate different performance parameters. This is known as “front end” design. In industry, CAD tools are used to generate gate and transistor level design. If students have access to these tools, they are allowed to use them for the design of this project.

The following are the general design considerations:

- Refer to chapter 7.7 of your textbook to calculate W/L ratio for transient performance.
- To avoid clock skew, use drivers (2 inverters in series) before the clock goes to each flip-flop.
- Use input protection circuits (layout can be found on the class web site and Fig. 14.29 of the textbook) followed by a Schmitt trigger (can be found in Fig. 14.34 of the textbook) to all inputs coming from PAD contacts except Vdd and Vss.
- Use drivers (4 inverters in series) for all outputs connected to PAD contacts.
- Make sure to use at least one substrate contact and one well contact for every logic gate.

✓ SUGGESTED DESIGN STEPS:

1. Think about the logic of the design and prepare logical equations on the basis of the given conditions.
2. Design the gate level schematic by using logical equations and other logical conditions.
   Again check the functionality.
3. Using CMOS logic, design MOSFET level schematics for all logic gates.
4. Calculate aspect ratios for each and every MOSFET for its transient performance.
5. Calculate the mid voltage for each and every gate.
6. Calculate capacitances by using given parasitic capacitance values and equations to calculate capacitance.
7. Calculate rise time and fall time for each and every logic gate. Remember, the rise and fall time for each type of gate will be different if it is driving a different load (e.g. a 1x inverter driving one inverter will have a different rise and fall time that a 1x inverter driving an inverter and a NAND gate).
8. Prepare a floorplan for your layout including the position of all gates, plans for clock and supply distribution, pad locations, etc.

❖ **REPORT SUBMISSION:**

- The cover page should include the course name and section, name of instructor, name of project partners, SID, email address and date submitted.
- Show and explain all equations and methods used to calculate various parameters. You do not need to show the calculations for all types of gates, just explain the procedure.
- Prepare a table which shows all parameters and all calculated values.
- Report how you found aspect ratio for transient performance for different logic and complex gates.
- Include a gate level schematic of your design.
- Include transistor level schematics for all gates in your design, with W/L’s shown for all transistors. Note that you do not need to combine all transistors into one big sheet, instead prepare individual transistor level schematics for all hierarchical cells in your design.
- Include a floor plan for the layout of your design.
Phase – II: Layout Work (Due: May 10th, 2007, at the beginning of class)

In this phase students will learn how to prepare layout for mask creation. The layout must follow all design rules. The design rules are technology and fabrication dependent. Use the MORBN20.tdb file (which is what you used for project 1). The layout should be area optimized. The layout work is called the backend design. In L-Edit student version 7.12, we are allowed to use only 3,000 objects. You will not be able to save your work once you exceed this limit. You can count number of objects by using, “View -> Count Objects.” Use orthogonal routing techniques to minimize the number of objects. Use select all (ctrl + A) and see how you have laid out different polygons; try to combine small polygons into one large polygon using the “merge” command. Create all cells in separate files and instance them in one main file.

❖ LAYOUT CONSIDERATIONS:

- Make all devices as small as design rules allow, including placing NMOS and PMOS devices as close as possible and also make the routing as close as possible.
- First, use as many active contacts as possible without compromising area and later on if you run out of objects, remove extra active contacts.
- The PAD contacts are 10x10 λ. As shown in the above pin diagram, several PAD contacts are on the left side and several are on the right side.

❖ ROUTING:

- Make sure to use one Vdd bus for all Vdd connections and one Vss bus for all Vss connections.
- Make routing using metal1 and metal2 such that metal1 routes vertical and metal2 routes horizontal (limited exceptions are acceptable). Metal2 should be used for Vdd and Vss routing as much as possible.
- There should not be any inverted inputs. Use only inputs those are given in the design.
- The resistance of poly is higher than metal 1 and the resistance of metal 1 is higher than metal 2. So, use metal 2 for power connections and extra long connections, metal 1 for long connections and poly for short connections.
- To carry necessary current, the power supply and ground busses should be wider when they are nearer to PAD contacts than center of the chip.

❖ SUGGESTED LAYOUT STEPS:

1. Open the layout editor tool and change the environment into 256 colors. First of all, set grids by selecting “setup > design > grid” to 1.0. This set up does not allow you to work in between grids. This is because our design specification says that our unit equal to one grid equal to 1 µm.
2. Think about hierarchical design. Each block of the floor plan should contain some number of cells. The cell partition is also on the basis of repetitive work in the design. Use different files to generate these cells rather than using different cells in one file. These will help to minimize the number of objects.
3. While making layout, do not forget to use substrate contacts and follow routing rules.
4. Clear DRC errors in each and every file.
5. In the main layout, follow the floor plan from left to right starting from the input PAD contacts, input protection circuit, Schmitt trigger, combinational circuits, clock driver, sequential circuits, output driver and output PAD contacts.

6. Instantiate all these files in a main layout in the same order. Don’t instantiate all files at a time. Place and route properly so that the final layout consumes less area. Check DRC errors before any new instantiation. Use “cut/copy + paste” technique for repetitive work in the same layout.

7. Verify again by comparing the layout with the floor plan.

8. Take the cross sections of each gate type: one from the center of “active contact” of PMOS and another from the center of “active contact” of NMOS.

FINAL REPORT SUBMISSION:

Please make sure your submissions are legible. Handwritten or hand drawn submissions are not valid. You will be graded on the professionalism of your submission. The completed project should include the following, in order:

- The cover page should include the course name and section, name of instructor, name of project partners, SID, email address and submission date.
- Table of contents
- A brief write up at least for (1) logic of the design (2) design aspects along with design calculations, (3) fabrication aspects from a cross section point of view (4) design flow: both front end and back end (5) contribution of project partners
- A state diagram if it is applicable
- A floor plan of the layout.
- A gate level schematic of the design with each gate and node labeled.
- A transistor level schematic of each logic gate in the design, with W/L’s clearly shown besides each associated device.
- A color print out of layout for Flip Flop. You can also put other small designs which are used for main layout.
- A color print out of whole layout.
- A cross section of layout. To take print out of the cross section view, use the “Print Screen” key of a keyboard. Then paste it into word document.
- A print out of the final DRC report.
- Conclusion: what you have learned in this project.
- Soft copy of all work in either CD or floppy disk; however, CD will be preferable. Do not send via email.

PARTNERSHIP AND PLAGIARISM:

Students can work together with a maximum of two students per group. To avoid plagiarism, the file names should contain both partners’ last name followed by course name and ‘proj2’. For example, if Smith and Patel are project partners then file names should include cpe151proj2_Smith_Patel. To differentiate layout and schematic files, you can add short form such as lo for layout, ld for logic diagrams, sc for transistor schematic as a suffix with above name. Also write project partners’ names in layouts and schematics.