For each of the following questions, choose the best response. (2 points each)

1. As $V_{ds}$ is increased above $V_{gs} - V_t$ in an NMOS FET, which of the following increases?
   a) the voltage across the channel
   b) the length of the channel
   c) the width of the depletion region surrounding the drain PN junction
   d) the width of the depletion region surrounding the source PN junction
   e) all of the above

2. If a CMOS inverter has $V_{in} = V_{out}$, in what regions of operation are the PMOS and NMOS devices?
   a) the PMOS is in triode, and the NMOS is in triode
   b) the PMOS is in triode, and the NMOS is in saturation
   c) the PMOS is in saturation, and the NMOS is in triode
   d) the PMOS is in saturation, and the NMOS is in saturation
   e) none of the above

3. As the number of dopant atoms in a region of silicon is increased, the conductivity will:
   a) increase
   b) stay constant
   c) decrease
   d) indeterminate
   e) none of the above

4. Which of the following materials used in CMOS processing is used to passivate the finished chip?
   a) silicon dioxide
   b) silicon nitride
   c) polysilicon
   d) aluminum
   e) none of the above.

5. According to ideal scaling theory, as FETs are scaled down which of the following will decrease:
   a) threshold voltage
   b) supply voltage
   c) gate oxide thickness
   d) transit time
   e) all of the above

6. According to ideal scaling theory, as a MOSFET is scaled down the electric fields will:
   a) increase
   b) stay constant
   c) decrease
   d) indeterminate
   e) none of the above
7. The gate-to-channel voltage in a saturated FET is:
   a) the same everywhere in the channel
   b) higher at the drain end of the channel
   c) higher at the source end of the channel
   d) indeterminate
   e) none of the above

8. FET drain-to-source leakage currents are caused by:
   a) sub-threshold slope
   b) hot electron effects
   c) quantum mechanical tunneling
   d) PN junction leakage
   e) all of the above

9. Which of the following is not true for a symmetric CMOS inverter?
   a) $\beta_N = \beta_P$
   b) $V_{MIDPOINT} = V_{DD}/2$
   c) $t_{RISE} = t_{FALL}$
   d) $W/L_P > W/L_N$
   e) none of the above

10. “Field implants” are used in CMOS processes to:
    a) control the threshold voltage of FETs
    b) prevent latch-up by reducing the $\beta$ of parasitic BJTs
    c) reduce the possibility of damage during an ESD event
    d) prevent parasitic FETs from turning on
    e) all of the above

For each of the following, choose either: a) True or b) False (2 points each)

11. Epitaxial layers are often used to reduce substrate resistance.
12. Standard cell libraries often include logic gates based on CMOS transmission gates to increase speed.
13. To reduce capacitance between metal lines, deep sub-micron CMOS processes have switched from silicon dioxide to high-K dielectrics to insulate between metal layers.
14. Deep sub-micron CMOS processes use copper instead of aluminum to reduce metal resistance.
15. Most standard CMOS logic gates are designed to have symmetric rise and fall times.
16. An AOI gate used as an XOR can be changed to an XNOR just by reconnecting its inputs.
17. To implement an “and” function in a complex CMOS gate, the PMOS FETs are placed in parallel.
18. If both a NAND and a NOR gate drive equal load capacitances, the NAND will use more power.
19. Flip-chip packaging offers better performance for high-speed chips, but costs more than standard packages using bond wires.
20. Drain Induced Barrier Lowering (DIBL) causes threshold voltage to increase as $V_{DS}$ increases.
For each of the following questions, choose the best response. (6 points each)

For questions 21 – 28 below, use the following values for a 0.25µm CMOS process:
\( V_{DD} = 2.5V, \quad k'_N = 180\mu A/V^2, \quad k'_P = 80\mu A/V^2, \quad V_{TN} = |V_{TP}| = 0.50V, \quad \text{all diffusion lengths} = 1\mu m, \)
\( L_{\text{overlap}} = 0.05\mu m, \quad C_{OX} = 8fF/\mu m^2, \quad C_{jn} = C_{jp} = 1fF/\mu m^2, \quad C_{jswa} = C_{jswp} = 0.5fF/\mu m \)

21. An inverter with \( W/L_P = W/L_N = 2/0.25 \) will have a midpoint voltage of:
   a) 1.8 V  
   b) 1.5 V  
   c) 1.3 V  
   d) 1.1 V  
   e) 1.0 V  

22. The output capacitance, \( C_{FET} \), of this inverter is:
   a) 12 fF 
   b) 14 fF 
   c) 18 fF 
   d) 20 fF 
   e) 24 fF 

23. The resistance of the FET that is on when the output of this inverter is pulling high is:
   a) 1550 Ω 
   b) 1130 Ω 
   c) 780 Ω 
   d) 570 Ω 
   e) 350 Ω 

24. If the total capacitance this inverter must drive including its load is 50fF, the 10-90% fall time is:
   a) 86 ps 
   b) 76 ps 
   c) 59 ps 
   d) 43 ps 
   e) 38 ps 

25. How much power would this inverter use if it drove a load of 100fF at 400MHz?
   a) 250 µW 
   b) 175 µW 
   c) 100 µW 
   d) 75 µW 
   e) 25 µW 

26. How much drain current will flow in the FETs if this inverter is biased with \( V_{in} = 1.0V \)?
   a) 80 µA 
   b) 90 µA 
   c) 160 µA 
   d) 180 µA 
   e) 210 µA
27. A 3-input NAND with $W/L_P = W/L_N = 2/0.25$ for all FETs will have a midpoint voltage of:
   a) 2.0 V  
   b) 1.7 V  
   c) 1.5 V  
   d) 1.2 V  
   e) 1.0 V

28. If this 0.25µm CMOS process is scaled to 0.13µm, the threshold voltage would ideally scale to:
   a) 260 mV  
   b) 320 mV  
   c) 440 mV  
   d) 500 mV  
   e) 960 mV

29. In the figure at right, the small n- diffusions next to the gate are:
   a) silicide to reduce drain/source resistance
   b) lightly doped drains
   c) depletion regions
   d) field implants
   e) none of the above

30. The logic function implemented by the layout shown at right is:
   a) $F = z \cdot x \cdot (y + w)$
   b) $F = w + y + (z \cdot x)$
   c) $F = w \cdot y \cdot (z + x)$
   d) $F = w \cdot y \cdot (z + x)$
   e) $F = z \cdot x \cdot (y + w)$

**BONUS (6 points):**

31. Which of the following is **not** a problem with scaling current CMOS processes to smaller sizes?
   a) increasing gate leakage
   b) increasing resistance of metal lines
   c) increasing capacitance of metal lines
   d) creating structures smaller than the wavelength of the light used to expose the masks
   e) none of the above