For each of the following questions, choose the best response. (2 points each)

1. If an NMOS FET is biased with $V_{gs} \ll 0$ and $V_{ds} > V_{gs} - V_t$, the device is in :
   a) cutoff
   b) triode
   c) saturation
   d) accumulation
   e) none of the above

2. As $|V_{ds}|$ is increased above $|V_{dsat}|$ for a PMOS FET :
   a) the voltage across the channel increases
   b) the depletion region around the drain gets wider
   c) the channel becomes “pinched-off” near the source
   d) the capacitance of the drain PN junction gets larger
   e) all of the above

3. Design rules are used when drawing the layout for a circuit to :
   a) prevent metal and poly lines from having shorts or opens
   b) avoid defects due to alignment errors between masks
   c) keep PN junction depletion regions from merging
   d) prevent drain-source shorts
   e) all of the above

4. If the thickness of a doped region of silicon is increased while the doping levels are kept constant, the sheet resistance of this region will :
   a) increase
   b) stay constant
   c) decrease
   d) indeterminate

5. Which of the following is used to lower the resistance of sources and drains?
   a) silicide
   b) polysilicon
   c) silicon dioxide
   d) silicon nitride
   e) none of the above

6. According to ideal scaling theory, which of the following stays constant as a CMOS process is scaled down to smaller dimensions?
   a) the transit time
   b) the process transconductance, $k’$
   c) the current through an FET in triode
   d) the resistance of an “on” MOS switch
   e) none of the above.
7. A CMOS inverter with $V_{TN} = |V_{TP}|$ and a midpoint voltage that is > $V_{DD}/2$ has:
   a) $\beta_N/\beta_P < 1$
   b) $\beta_N/\beta_P = 1$
   c) $\beta_N/\beta_P > 1$
   d) indeterminate

8. A CMOS inverter with $V_{TN} = |V_{TP}|$ and equal 10-90% rise and fall times has:
   a) $\beta_N/\beta_P < 1$
   b) $\beta_N/\beta_P = 1$
   c) $\beta_N/\beta_P > 1$
   d) indeterminate

9. For the CMOS 2-input NAND gate shown at right, the lowest midpoint voltage will occur when:
   a) Input A and input B are switched simultaneously
   b) Input A is tied to $V_{DD}$ and input B is switched from 0 to $V_{DD}$
   c) Input B is tied to $V_{DD}$ and input A is switched from 0 to $V_{DD}$
   d) indeterminate

10. Which of the following will not increase the power used by a CMOS logic gate?
    a) Increasing the fan-out
    b) Increasing the supply voltage
    c) Increasing the clock frequency
    d) Increasing the activity factor
    e) Increasing the number of FETs in the gate

For each of the following, choose either: a) True or b) False (2 points each)

11. Sub-threshold leakage increases as threshold voltage increases due to quantum mechanical tunneling.
12. With copper metal, Chemical Mechanical Polishing is applied directly to the copper.
13. Thick FOX and field implants are both used to keep unwanted parasitic FETs turned off.
14. Body effect causes the current through an FET to increase as it’s source-to-bulk voltage increases.
15. Lightly doped drains reduce hot electron effects in FETs by reducing electric field strengths.
16. Symmetric inverters use larger PMOS FETs than NMOS since holes are more mobile than electrons.
17. A logic gate’s fan-out refers to how many identical logic gates a particular gate drives.
18. Oxide erosion refers to a problem which can occur if an aluminum line is over-etched.
19. As the implanted dose is increased, the resistance of the resulting silicon will decrease.
20. Most digital cell libraries use gates with symmetric VTCs since this is critical to digital circuits.
For each of the following questions, choose the best response. (6 points each)

21. In the figure shown at right, the striped areas shown touching either side of the gate are:
   a) silicide to reduce gate resistance
   b) oxide spacers
   c) lightly doped drains
   d) silicon nitride
   e) none of the above

22. The circuit shown at right implements the logic equation:
   a) \( F = (a \cdot b \cdot c) + (b \cdot d) \)
   b) \( F = a \cdot (b + c) + b \cdot d \)
   c) \( F = (a+b \cdot c) \cdot (b+d) \)
   d) \( F = a \cdot (b+c) + b \cdot d \)
   e) none of the above

23. If the resistance of a polysilicon line 2\(\mu\)m wide and 100\(\mu\)m long is measured to be 600 Ohms, the sheet resistance must be:
   a) 12 Ohms
   b) 10 Ohms
   c) 8 Ohms
   d) 6 Ohms
   e) none of the above

24. Find the drain current for an NMOS FET with \(V_{gs} = V_{ds} = 2.0V\).
   Use: \(V_{TN} = 0.6V, k'_N = 125\mu A/V^2, \lambda_N = 0, W/L = 10\)
   a) \(I_d = 2.50\ mA\)
   b) \(I_d = 2.00\ mA\)
   c) \(I_d = 1.25\ mA\)
   d) \(I_d = 1.00\ mA\)
   e) \(I_d = 0.75\ mA\)

25. Find the drain current for a PMOS FET with \(V_{gs} = -3.0V\) and \(V_{ds} = -1.4V\).
   Use: \(V_{TP} = -0.5V, k'_P = 40\mu A/V^2, \lambda_P = 0, W/L = 5\)
   a) \(I_d = 1250\ \mu A\)
   b) \(I_d = 900\ \mu A\)
   c) \(I_d = 750\ \mu A\)
   d) \(I_d = 625\ \mu A\)
   e) \(I_d = 500\ \mu A\)

26. The midpoint voltage of a 3-input NAND gate using \(W/L_N = 9/1\) and \(W/L_P = 3/1\) is:
   Assume simultaneous switching, \(V_{DD} = 3.0V, V_{TN} = |V_{TP}| = 0.5V, k'_N = 120\mu A/V^2, k'_P = 40\mu A/V^2\).
   a) 1.0 V
   b) 1.2 V
   c) 1.5 V
   d) 1.8 V
   e) 2.0 V
27. When the inverter pulls its output high, the resistance of the FET that is ON is:
   a) 5.0 kΩ
   b) 2.5 kΩ
   c) 1.7 kΩ
   d) 1.3 kΩ
   e) 1.0 kΩ

28. The capacitance on the output node from this inverter alone (without an external load) is:
   a) 37 fF
   b) 28 fF
   c) 21 fF
   d) 17 fF
   e) 8 fF

29. If the total capacitance on the output node is 40 fF, the 10-90% rise time will be:
   a) 220 psec
   b) 180 psec
   c) 150 psec
   d) 110 psec
   e) 90 psec

30. If this inverter drives a fan-out of 4, its 10-90% fall time will be:
   a) 340 psec
   b) 285 psec
   c) 250 psec
   d) 210 psec
   e) 175 psec

31. BONUS: (6 points) By what percent would the W/L of the PMOS FET in the inverter above have to be increased to make the inverter have equal rise and fall times?
   a) 0 %
   b) 25 %
   c) 33 %
   d) 50 %
   e) 100 %