For each of the following questions, choose the best response. (2 points each)

1. Timing analysis is typically done after each of the following steps, except:
   a) Creation of the RTL code
   b) Synthesis of the gate level netlist
   c) Place and route of the layout
   d) Clock tree insertion
   e) None of the above

2. Flip-flops with short clock-to-Q delays are desirable, but can lead to:
   a) Setup time violations
   b) Hold time violations
   c) Both setup and hold time violations
   d) Neither setup or hold time violations
   e) None of the above

3. Setup time violations can be caused by:
   a) Too many logic gates placed between registers.
   b) Large clock skews.
   c) Large flip-flop clock-to-Q delays.
   d) Large flip-flop setup times.
   e) All of the above.

4. The type of IC testing which uses alternate data and clock inputs to flip-flops is:
   a) IDDQ
   b) JTAG
   c) SCAN
   d) Functional
   e) None of the above

5. Which of the following advanced CMOS techniques is the most widely used?
   a) Mirror circuits
   b) Pseudo-NMOS logic
   c) Dynamic logic
   d) Tri-state logic
   e) None of the above

6. Which of the following advanced CMOS techniques is the most vulnerable to crosstalk?
   a) Mirror circuits
   b) Pseudo-NMOS logic
   c) Dynamic logic
   d) Tri-state logic
   e) None of the above
7. In an SRAM array, bits are often interdigitated between words to:
   a) Reduce capacitance on the word lines
   b) Increase symmetry in the core layout
   c) Improve the aspect ratio of the core layout
   d) Ease routing for the column MUX’s
   e) All of the above

8. Which of the following reliability problems are tested by burn-in?
   a) Infant mortality
   b) Random failures
   c) Wear-out failures
   d) None of the above
   e) All of the above

9. Sense amplifiers are needed in DRAMs because:
   a) The small FETs in the bit cell are slow to pull the bit lines all the way to Vdd or ground
   b) Charge sharing only changes the bit line voltages a small amount
   c) Using them saves power
   d) Using them increases speed
   e) All of the above

10. Input pads typically include which of the following for ESD and latchup protection?
    a) Resistors
    b) Diodes
    c) Field-oxide FETs
    d) Snap-back devices
    e) All of the above

For each of the following, choose either: a) True or b) False (2 points each)

11. Schmitt triggers are often used on input signals to prevent false switching due to noise.
12. E²PROMs store data using trapped charge on floating gates to increase hot electron effects.
13. Ground bounce occurs more with flip chip packaging than with packages using bond wires.
14. Ground bounce occurs on both ground and Vdd power supplies.
15. A multiplication by 2 can be performed simply by shifting the bits in a word left by 1 position.
16. Ripple-carry adders are both smaller and faster than carry look-ahead adders.
17. Barrel shifters select only N bits out of an M bit word to send to the output.
18. Toggle flip-flops are really just D flip-flops with the D input connected to the Q output.
19. In a NAND-based R/S latch, the set and reset inputs are active low.
20. The best way to add load control to a flip-flip is to AND the clock with a load control bit.
For each of the following questions, choose the best response. (6 points each)

21. A VLSI designer plans to pipeline a data path using D-type flip-flops with $t_{\text{clk-to-Q}} = 75$ psec, $t_{\text{setup}} = 100$ psec and $t_{\text{hold}} = 150$ psec. If a 1 GHz clock is used with a maximum clock skew of 125 psec, and the worst case gate delay is 75 psec, then what is the maximum number of logic gates that can be used between flip-flops?
   a) 8
   b) 9
   c) 10
   d) 11
   e) 12

22. If the flip-flops in problem 21 are used to build a shift register, what is the minimum number of inverters that must be used between each flip-flop?
   a) 0
   b) 1
   c) 2
   d) 3
   e) 4

23. If a circuit is built using the flip-flops in problem 21 with 8 logic gates between each flip-flop, what is the timing margin for setup time analysis?
   a) 50 psec
   b) 75 psec
   c) 100 psec
   d) 200 psec
   e) 225 psec

24. If the clock used in problem 21 is decreased to 750 MHz and 2 logic gates are used between each flip-flop, what is the timing margin for hold time analysis?
   a) 100 psec
   b) 50 psec
   c) 0 psec
   d) -50 psec
   e) -100 psec

25. If a 101 stage ring oscillator is built from inverters with a gate delay of 75 psec, at what frequency will it oscillate?
   a) 66 MHz
   b) 78 MHz
   c) 91 MHz
   d) 104 MHz
   e) 132 MHz
26. A DRAM cell uses a storage capacitor of 25 fF, $V_{DD} = 1.8V$ and $V_T = 0.4V$ for the NMOS access FET. If $I_{leakage} = 500$ pA, the bit line capacitance is 225 fF, and the time between refresh cycles is 50µsec, what voltage must the sense amp be able to detect as a valid one?

a) $20 \text{ mV}$
b) $40 \text{ mV}$
c) $80 \text{ mV}$
d) $100 \text{ mV}$
e) $120 \text{ mV}$

27. In the E²PROM shown at right, what code is stored in this word?

a) 01011001
b) 01101001
c) 10101010
d) 10010110
e) none of the above

28. If a 3-input NOR gate has $\beta_N = \beta_P$, $V_{DD} = 2.5V$ and $|V_{TP}| = V_{TN} = 0.35V$, the midpoint voltage for simultaneous switching is:

a) 1.25 V
b) 1.00 V
c) 0.80 V
d) 0.50 V
e) 0.35 V

29. To achieve equal worst case rise and fall times in the complex logic gate shown at right, the W/L's of the PMOS FETs connected to the w and y inputs must be increased by what factor? Assume all other FETs are minimum size and $k'_{N} = 3 \cdot k'_{P}$.

a) 2x
b) 3x
c) 4x
d) 6x
e) none of the above

30. A clock is routed from a clock generator to 2 circuit blocks which are 200µm and 500µm away. Find the skew between the clocks after they arrive at the blocks. Assume identical wires are used with $W = 0.5\mu m$, $t = 0.7\mu m$ and $Rs = 0.1 \Omega/\square$. The metal runs over field oxide 1µm thick.

a) 10.8 psec
b) 9.7 psec
c) 7.2 psec
d) 4.5 psec
e) 2.3 psec

31. **BONUS**: (6 points) If fringe capacitance were neglected in problem 30, the skew would be:

a) higher  
b) the same  
c) lower  
d) indeterminate  
e) none of the above