For each of the following questions, choose the best response. (2 points each)

1. If a CMOS inverter is biased with $V_{\text{in}}$ equal to the inverter’s midpoint voltage, in what regions of operation are the PMOS and NMOS devices?
   a) the PMOS is in triode, and the NMOS is in triode
   b) the PMOS is in triode, and the NMOS is in saturation
   c) the PMOS is in saturation, and the NMOS is in triode
   d) the PMOS is in saturation, and the NMOS is in saturation
   e) none of the above

2. To create a symmetric VTC for a CMOS inverter requires that:
   a) the ratio of $W/L_P$ to $W/L_N$ be set = 1
   b) the ratio of $W/L_P$ to $W/L_N$ be set = the ratio of $V_{TP}$ to $V_{TN}$
   c) the ratio of $W/L_P$ to $W/L_N$ be set = the ratio of $k'_P$ to $k'_N$
   d) the ratio of $W/L_P$ to $W/L_N$ be set = $V_{DD}/2$
   e) none of the above

3. To calculate the rise time of a CMOS inverter, which of the following terms should not be included?
   a) the capacitance of the PMOS and NMOS drain PN junctions
   b) the capacitance of the PMOS and NMOS source PN junctions
   c) the capacitance of the PMOS and NMOS gate oxides
   d) the load capacitance
   e) none of the above

4. For the case of simultaneous switching, a 2-input NOR gate looks like an inverter with:
   a) a PMOS FET with 2x the L and an NMOS FET with 2x the W
   b) a PMOS FET with 2x the W and an NMOS FET with 2x the L
   c) a PMOS FET with 2x the L and an NMOS FET with 1x the W
   d) a PMOS FET with 2x the W and an NMOS FET with 1x the L
   e) none of the above

5. As the fan-out of a CMOS logic gate increases, it’s propagation delay increases proportional to:
   a) the on-resistance of the PMOS FETs
   b) the on-resistance of the NMOS FETs
   c) the self-capacitance of the logic gate
   d) both a & c above
   e) both a & b above

6. The equation for the average power dissipated by a CMOS logic gate, $P_{\text{AVG}} = C_{\text{OUT}} \cdot V_{DD}^2 \cdot F_{\text{CLOCK}}$ neglects which of the following terms?
   a) leakage current
   b) shoot-through current
   c) activity factor
   d) all of the above
   e) none of the above
7. If the length of an interconnect line is cut in half, the delay through the line will:
   a) decrease by 25%
   b) decrease by 50%
   c) decrease by 75%
   d) decrease by 90%
   e) indeterminate

8. If the width of an interconnect line is cut in half, the delay through the line will:
   a) decrease by 25%
   b) decrease by 50%
   c) increase by 25%
   d) increase by 50%
   e) indeterminate

9. “Ground bounce” is caused by:
   a) bond wire and package lead resistance
   b) bond wire and package lead capacitance
   c) bond wire and package lead inductance
   d) a & b above
   e) none of the above

10. Schmitt Triggers are often used on input pads to prevent errors due to:
    a) noise
    b) latch-up
    c) electrostatic discharge
    d) hysteresis
    e) all of the above

For each of the following, choose either: a) True or b) False (2 points each)

11. Output pads often use “break-before-make” circuits to prevent large shoot-through currents.
12. Two major concerns when designing the supply distribution grid for an IC are IR drops and electromigration.
13. Clock trees often use minimum width interconnect lines to reduce delay through the lines.
14. Resistors, diodes and snap-back devices are often added to pads to prevent damage due to ESD.
15. Most gates in a typical CMOS digital standard cell library are sized to have a symmetric VTC.
16. Rotate left and right circuits are typically used to multiply and divide binary numbers by powers of 2.
17. Latches and flip-flops store data using bistable circuits based on positive feedback.
18. RTL code refers to the top-level behavioral model of a chip which only contains architectural details.
19. Timing analysis is usually only done after the initial place-and-route is complete to save design time.
20. Set and clear inputs are often built into flip-flops to allow the stored values to be initialized.
For each of the following questions, choose the best response. (6 points each)

For questions 21 – 25 below, use the following values for the 2-input CMOS NOR gate shown at right:

\[ V_{DD} = 2.5V, W_P = 3\mu m, W_N = 1\mu m, L_P = L_N = 0.25\mu m, \]
\[ k_N' = 180 \mu A/V^2, k_P' = 60 \mu A/V^2, V_{TN} = 0.5V, V_{TP} = -0.5V, \]
all diffusion lengths = 1\mu m, \( L_{overlap} = 0.1\mu m, C_{OX} = 8 \text{ fF/} \mu m^2, \]
\[ C_{jn} = C_{jp} = 1 \text{ fF/} \mu m^2, C_{jswn} = C_{jswp} = 0.5 \text{ fF/} \mu m, C_{load} = 25\text{fF} \]

21. The midpoint voltage for simultaneous switching is:
   a) 1.41 V
   b) 1.25 V
   c) 1.00 V
   d) 0.80 V
   e) 0.71 V

22. The total capacitance on the output node is:
   a) 15 fF
   b) 20 fF
   c) 25 fF
   d) 40 fF
   e) 45 fF

23. If the total capacitance on the output node was 50fF, the worst case 10-90% fall time would be:
   a) 35 psec
   b) 76 psec
   c) 88 psec
   d) 98 psec
   e) 102 psec

24. If the total capacitance on the output node was 50fF, the worst case 10-90% rise time would be:
   a) 75 psec
   b) 128 psec
   c) 153 psec
   d) 165 psec
   e) 176 psec

25. If the worst case 10-90% rise time = 135 psec and fall time = 85 psec, the propagation delay is:
   a) 35 psec
   b) 70 psec
   c) 90 psec
   d) 110 psec
   e) 220 psec
26. The function performed by the complex CMOS logic gate shown at right is:
   a) \( a \cdot (b + c) \)
   b) \( \overline{a} \cdot (b + c) \)
   c) \( a + (b \cdot c) \)
   d) \( a + (b \cdot c) \)
   e) \( a + b + c \)

27. To equalize the worst-case rise and fall times of this gate, the NMOS W/L's must be increased by:
   a) 0.5 x
   b) 1.0 x
   c) 1.5 x
   d) 2.0 x
   e) 3.0 x

28. To equalize the worst-case rise and fall times, all the PMOS W/L’s must be increased except for the FETs connected to:
   a) \( a \)
   b) \( b \)
   c) \( c \)
   d) \( b \) and \( c \)
   e) \( a, b \) and \( c \)

29. An interconnect line has a resistance of 1 \( \Omega/\mu m \) and a capacitance of 0.1 fF/\( \mu m \). The time constant for 200\( \mu m \) of this line is:
   a) 1 psec
   b) 2 psec
   c) 4 psec
   d) 6 psec
   e) 8 psec

30. If the delay through 100\( \mu m \) of an interconnect line is 1psec, the delay through 1000\( \mu m \) of this line would be:
   a) 10 psec
   b) 20 psec
   c) 50 psec
   d) 100 psec
   e) 200 psec

31. **BONUS** (6 points): If a 101 stage ring oscillator is built out of CMOS inverters with gate delays of 99psec each, the frequency observed will be:
   a) 200 MHz
   b) 100 MHz
   c) 50 MHz
   d) 25 MHz
   e) 10 MHz