For the following questions, circle the best response. (20 points)

1. 4T SRAM cells with poly resistors are sometimes used instead of 6T SRAM cells because they are:
   - Faster
   - Cheaper
   - Smaller
   - Easier to design

2. In a memory, “word lines” are used for:
   - Data
   - Control
   - Clocks
   - Supplies

3. A type of memory which stores its values as charge on capacitors is:
   - SRAM
   - DRAM
   - ROM
   - E²PROM
   - PLA

4. Dynamic logic is sometimes used instead of standard CMOS logic because it is:
   - Faster
   - Cheaper
   - More robust
   - Easier to design

5. Dynamic logic suffers from all of the following except:
   - Leakage
   - Charge sharing
   - Crosstalk
   - Static power dissipation

6. Pipelining of data paths is used to increase all of the following except:
   - Clock frequency
   - Latency
   - Data throughput
   - Activity of logic gates

7. The maximum number of logic gates which can be placed between two registers is affected by all of the following except:
   - Clock period
   - Set-up time
   - Hold time
   - Clock skew
   - Clock-to-Q delay

8. If the supply voltage applied to a chip increases, ground bounce will get:
   - Larger
   - Smaller
   - Same
   - Indeterminate

9. “Scan” refers to a test methodology used to check the operation of:
   - Clock trees
   - Logic Gates
   - Output pads
   - Flip-Flops

10. “Burn-in” is performed on chips before shipping to reduce failures due to:
    - Wear-out
    - Random failures
    - Infant mortality
    - IDDQ failures
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Hand-shaking ________
12. PLL ________
13. Crosstalk ________
14. WAT key ________
15. H-trees ________

A. A layout technique used to reduce clock skew.
B. A key CMOS process parameter used in calculating the power dissipation of a chip.
C. A layout technique used to reduce ground bounce.
D. Noise due to inductive coupling through the silicon substrate.
E. Test structures added to the wafer to verify that a good process lot was obtained.
F. A complex analog circuit used in clock generation.
G. A method used to synchronize clocks from 2 or more chips.
H. Noise due to capacitive coupling between metal lines.
I. A complex analog circuit used for ESD protection.
J. A method used to transfer data without the need to synchronize clocks.
16. (20 points) A VLSI designer plans to pipeline a data path with a 200 MHz clock using D-type flip-flops with the following characteristics: $t_{\text{clk-to-Q}} = 300$ psec, $t_{\text{setup}} = 200$ psec, $t_{\text{hold}} = 100$ psec. If the longest logic chain between flip-flops is 16 gates, each with a worst-case gate delay of 250 psec, then what is the maximum amount of clock skew that can be tolerated? If a clock with this much skew is used, what is the minimum number of gates that must be placed in the shortest logic chain?
17. (20 points) A dynamic logic gate is shown below. (a) What is the logic equation for this gate? (b) If the inputs are \( abcy = 10101 \) on the first clock cycle when \( \Phi = 1 \), and then change to \( abcy = 10010 \) on the second clock cycle, what will the output voltage be when \( \Phi = 1 \) on the second clock cycle? Assume \( V_{DD} = 3V \), all nodes except the output have parasitic capacitances of 10fF on them, and the output drives a load capacitance of 50fF.
18. (20 points) Sketch the layout of a 6-T SRAM cell. Show all devices and metal interconnect, and label all inputs and outputs with their functions (including power supplies). Assume 3 metal layers are available in the process and label all metal lines M1, M2 or M3 to indicate which is used for each.
BONUS (5 points) List 5 items which must be considered when floorplanning a chip layout.