1. If the output of a VLSI block has less bits than its input, then the block’s function could be:
   - Rotate Left
   - Rotate Right
   - Shift Left
   - Shift Right
   - Barrel Shift

2. If a NOR gate is made with all minimum size MOSFETs, will the rise or fall time be faster?
   - Rise
   - Fall
   - Same
   - Indeterminate

3. If both a NAND gate and a NOR gate are made with all minimum size MOSFETs, which will have the faster fall time?
   - NAND
   - NOR
   - Same
   - Indeterminate

4. If both a NAND gate and a NOR gate are sized to have equal mid-point voltages for simultaneous switching, which will require less silicon area?
   - NAND
   - NOR
   - Same
   - Indeterminate

5. If both 2-input and 3-input NAND gates are made with all minimum size MOSFETs, which will have the larger mid-point voltage for simultaneous switching?
   - 2-input
   - 3-input
   - Same
   - Indeterminate

6. Carry look-ahead adders are often used instead of ripple carry adders because they are:
   - Smaller
   - Larger
   - Faster
   - Slower

7. Compared to an R/S latch made with NANDs, the number of MOSFETs needed to build an R/S latch with NOR gates is:
   - Larger
   - Smaller
   - Same
   - Indeterminate

8. Compared to the device transconductance of an NMOS FET, the device transconductance of a PMOS is:
   - Larger
   - Smaller
   - Same
   - Indeterminate

9. The power used by CMOS circuits scale proportional to:
   - Clock frequency
   - Supply voltage
   - Area
   - Temperature

10. For a CMOS digital logic gate, circle which of the following will be the lowest voltage:
    - \( V_{IH} \)
    - \( V_{OL} \)
    - \( V_{IL} \)
    - \( V_{OH} \)
For the following questions, choose the best definition for each word or phrase. (20 points)

11. synthesis ________
12. propagate ________
13. RTL ________
14. P&R ________
15. Elmore rule ________

A. The term in a carry-look-ahead adder which determines if a new carry bit is created.
B. A method used to automatically layout digital standard cells.
C. A method used to calculate the rise and fall times of a complex CMOS logic gate.
D. The high-level digital code which specifies data storage and movement.
E. A method used to automatically generate transistor-level schematics for standard cells.
F. A method used to automatically generate gate-level schematics for digital blocks.
G. A method used to calculate the power used by a complex CMOS logic gate.
H. The term in a carry-look-ahead adder which determines if the carry-in is passed out.
I. The high-level digital code which specifies architectural details of a system.
J. A method used to assemble the layout of a digital block based on standard cells.
16. (20 points) For the inverter shown below: a) calculate the rise time, fall time and gate delay with $C_{\text{load}} = 0$, b) sketch a plot of gate delay vs $C_{\text{load}}$ showing delays for fan-outs from 0 to 10.

Use $W_P = 3 \mu m$, $W_N = 1 \mu m$, $L_P = L_N = 0.5 \mu m$, all diffusion lengths = $1 \mu m$, $L_{\text{overlap}} = 0.1 \mu m$, $V_{\text{DD}} = 3 V$, $C_{\text{OX}} = 5 fF/\mu m^2$, $k'_N = 120 \mu A/V^2$, $k'_P = 40 \mu A/V^2$, $V_{\text{TN}} = 0.6 V$, $V_{\text{TP}} = -0.6 V$, $C_{\text{jin}} = C_{\text{jp}} = 1 fF/\mu m^2$, $C_{\text{jswn}} = C_{\text{jswp}} = 0.25 fF/\mu m$
(extra work space for problem 16)
17. (20 points) Draw the schematic for a complex CMOS logic gate implementing the function 
\[ Y = (A+B+C)(D+E) \overline{F} \]  
Indicate the relative \textbf{W/L ratios} required for all MOSFETs to equalize the worst case rise and fall times. Assume \( \mu_N = 3 \mu_P \)
18. (20 points) Draw the gate-level schematic for a negative edge-triggered D-type flip-flop with reset using: a) T-gate switches, b) clocked inverters. Also draw the transistor-level schematic for your clocked inverter. Be sure to indicate on your schematics all clocks used.
BONUS (5 points) If the inverter in problem 16 is used to build a 51 stage ring oscillator, what will be the frequency of oscillation?