For the following questions, circle the best response. (20 points)

1. According to scaling theory, what happens to the electric fields in a FET as it is scaled down?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

2. According to scaling theory, what happens to the area of MOS circuits as they are scaled down?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

3. According to scaling theory, what happens to the k' of a FET as it is scaled down?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

4. What happens to the conductance of doped silicon as the doping concentration increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

5. What happens to the effective channel length in a FET as Vds increases beyond Vgs-Vt?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

6. What happens to the capacitance of a PN junction as the reverse bias increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

7. What happens to the gate capacitance of a FET with Vgs > Vt as the substrate doping increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

8. What happens to the magnitude of a FET threshold voltage as the gate oxide thickness increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

9. What happens to the channel resistance of a triode MOSFET as Vgs-Vt increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

10. What happens to the gate-to-channel voltage in a saturated FET as you move from source to drain?
    - Increases
    - Decreases
    - No Change
    - Indeterminate
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Silicide
   A. The process through which each mask is aligned to the features created by the prior mask.
   B. The process by which source and drain resistances are lowered using refractory metals.

12. Electromigration
   C. The effect which causes some drain current to flow into the substrate at high values of Vds.
   D. The effect which causes metal atoms to move due to high current densities.

13. Annealing
   E. The process used to pattern copper metal.
   F. The effect which causes drain current to increase as Vds is increased > Vgs – Vt.

14. Silicon Nitride
   G. The material used to define the pattern made in an SiO2 layer during etching.
   H. The process used to repair damage to the silicon crystal caused by ion implantation.

15. Dual Damascene
   I. The process used to planarize each interconnect layer before the next one is added.
   J. The material used to passivate a finished chip.
16. (20 points) Sketch the cross-section of a PMOS FET in saturation. Label all capacitances and give approximate equations for their values.

**NOTES:**
1) $C_{GS} =$ SMALL GAP IN DIAGRAM ABOVE FROM POLYSi GATE TO CHANNEL (HARD TO SEE - SORRY!)
2) $\text{N WELL, PSiV CONTACTS NOT SHOWN}$

**APPROX VALUES:**

- $C_{GS} = \frac{2}{3} \frac{C_{OX} \cdot W \cdot L}{} \quad \text{(Source)}$
- $C_{GD} = \frac{C_{OX} \cdot W \cdot \text{LOV}}{\text{(Overlap of Drain and Gate)}}$
- $C_{SB, PB, SBW, DBW} \text{ ARE ALL P-N JUNCTION}$
- $C_{APS} = \text{OF THE FORM: } \quad C_{j} = \frac{C_{j0} + \frac{V_{D}}{\delta_{j0}}}{\sqrt{1 + \frac{V_{D}}{\delta_{j0}}}}$

WHERE: $C_{j0}, \delta_{j0} \text{ VARY FOR EACH}$

BASED ON DOPING
17. (20 points) Calculate the threshold voltage for an NMOS FET at 27°C with (a) $V_{DD} = 1V$ and 
(b) $V_{DD} = 3V$. Use $V_{TH} = 0.5V$, $t_{ox} = 100\AA$ and $N_A = 1.6 \times 10^{12}/cm^2$.

Use:  
\[ V_T = V_{TH} + \gamma (\sqrt{2|\phi_F| + V_{SS}} - \sqrt{2|\phi_F|}) \]

\[ \gamma = \frac{2qN_x \phi_F}{C_{ox}} \quad |\phi_F| = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) \quad C_{ox} = \frac{e_{ox}}{t_{ox}} \]

\[ n_i \sim 10^{10}/cm^3 \quad q = 1.6 \times 10^{-19} \quad e_{ox} = 3.45 \times 10^{-12} \quad \mu F/cm \]
\[ e_S = 1.04 \times 10^{-12} \mu F/cm \]
\[ k = 1.38 \times 10^{-23} \mu V/K \]

\[ \text{1ST, FIND } \phi_F \text{ AND } \gamma \text{!} \]
\[ |\phi_F| = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) = \frac{(1.38 \times 10^{-22})(297)}{(1.6 \times 10^{-19})} \ln \left( \frac{1.6 \times 10^{12}}{10^9} \right) = 37 \mu V \]
\[ \Rightarrow 2|\phi_F| = 74 \mu V \]
\[ \gamma = \frac{2qN_x e_S}{C_{ox}} = \frac{2(1.6 \times 10^{12})(1.6 \times 10^{16})(1.04 \times 10^{-12})}{3.45 \times 10^{-12}} = 0.211 \mu V \]

\[ \gamma = \phi_F \text{, } 211 \mu V \]

\[ \text{NOW, } V_T = V_{TH} + \gamma \left( \sqrt{2|\phi_F| + V_{SS}} - \sqrt{2|\phi_F|} \right) \]

\[ a) \text{ WITH } V_{SS} = 1 \mu V \Rightarrow \]
\[ V_T = 0.5 \pm 0.211 \left( \sqrt{0.74} - \sqrt{0.74} \right) \]
\[ V_T = 597 \mu V \]

\[ b) \text{ WITH } V_{SS} = 3 \mu V \Rightarrow \]
\[ V_T = 0.5 \pm 0.211 \left( \sqrt{0.74+3} - \sqrt{0.74} \right) \]
\[ V_T = 727 \mu V \]
18. (20 points) In order, list the steps in a basic CMOS process flow through metal 1.

START WITH SILICON WAFER (USUALLY WITH EPI FOR DIGITAL)

THEN:

1) CREATE N-WELL REGIONS (MASK STEP)
2) DEFINE ACTIVE AREAS USING NITRIDE & "PAP OXIDE"
3) ETCH TRENCHES IN SILICON FOR BOX (FIELD OXIDE)
4) DEPOSIT FOX & PATTERN
5) REMOVE NITRIDE & PAP OXIDE TO PREPARE Si SURFACE (ACTIVE AREAS ARE NOW READY TO BUILD MOSFETS)
6) GROW GATE OXIDE
7) DEPOSIT POLY-Si AND ETCH TO PATTERN GATES
8) APPLY PHOTORESIST TO SHEILD AREAS FOR NMOS FETS & PATTERN, THEN IMPLANT P+ SOURCE/DRAINS USING PSELECT MASK
9) APPLY PHOTORESIST TO SHEILD AREAS FOR PMOS FETS & PATTERN USING NSELECT MASK, THEN IMPLANT N+ SOURCE/DRAINS
10) ANNEAL WAFER TO REPAIR CRYSTAL DAMAGE AFTER IMPLANTS
11) DEPOSIT SiO$_2$ FOR INTER-LAYER DIELECTRIC BETWEEN Si SURFACE AND METAL 1
12) PHOTORESIST STEP (MASK) TO PATTERN & ETCH CONTACTS TO GATE, SOURCE, DRAINS (ALSO WELL & SUB CONTACTS)
13) FILL CONTACTS WITH TUNGSTEN (W) OR OTHER METAL (SPECIFIC)
14) DEPOSIT AL AND PATTERN WITH ETCH MASK FOR METAL 1

OR,

14) ETCH GROOVES IN SiO$_2$ TO FORM METAL 1 PATTERN, FILL WITH COPPER (Cu) AND APPLY CMP TO REMOVE UNWANTED Cu (CMP = "CHEMICAL MECHANICAL POLISHING")
BONUS (5 points) Sketch 2 examples of layout design rules and explain why each is needed.

1) 

N+ diffusion must surround contact by some minimum spacing to avoid contact touching P-substrate if masks are mis-aligned.

2) 

Minimum extension ("overhang") of poly gate required outside edge of active area to avoid drain-source short if masks are mis-aligned.

Many more design rules exist.