DC CHARACTERISTICS OF CMOS INVERTERS

Figure 7.1 The CMOS inverter circuit

- **KEY PARAMETERS**: $V_{TN}, V_{TP}$ \{DEFINED BY PROCESS\}
  
  $k_n', k_p', \frac{W}{L}_n, \frac{W}{L}_p$ \{UNDER CONTROL OF DESIGNER\}

Figure 7.2 $V_{OH}$ and $V_{OL}$ for the inverter circuit

$V_{OH} = \text{"OUTPUT HIGH LEVEL"}$ \hspace{1cm} $V_{OH} = V_{DD}$ \{FOR CMOS INVERTER\}

$V_{OL} = \text{"OUTPUT LOW LEVEL"}$ \hspace{1cm} $V_{OL} = \emptyset$

$\text{"LOGIC SWING" = } V_{OH} - V_{OL} = V_{DD} = \text{"FULL-RAIL OUTPUT"}$

or

$\text{"RAIL-TO-RAIL OUTPUT"}$
Figure 7.3 Voltage transfer curve for the NOT gate

- $V_{TC} = \text{PLOT OF VOUT VS VIN AT DC (SLOWLY VARYING INPUT VOLTAGE)}$
- INVERTING CHARACTERISTIC
- $\text{V}_{OH} = V_{DD}$, $\text{V}_{OL} = 0 \}$ OUTPUT HIGH, LOW LEVELS

NOW, WHAT ABOUT INPUT HIGH, LOW LEVELS?

→ NEED TO DEFINE THE MAX VIN CONSIDERED A "0"
→ NEED TO DEFINE THE MIN VIN CONSIDERED A "1"

→ USE POINTS ON VTC WHERE SLOPE $= 1$

$\text{V}_{IL} = \text{INPUT LOW VOLTAGE} = \text{VIN AT POINT A}$ $\}$ $\phi, \overline{0}$ ARE WHERE SLOPE $= -1$

$\text{V}_{IH} = \text{INPUT HIGH VOLTAGE} = \text{VIN AT POINT B}$ $\}$ $\phi, 1$ ARE WHERE SLOPE $= -1$

BY DEFINITION:

$\text{V}_{IL} \geq \text{VIN} \geq \phi \}$ A VALID "0"

$V_{PP} \geq \text{VIN} \geq \text{V}_{IH} \}$ A VALID "1"

NOISE MARGINS:

$\text{VNMH} = \text{V}_{OH} - \text{V}_{IH}$

$\text{VNMH} = \text{V}_{IL} - \text{V}_{OL}$
CALCULATION OF MIDPOINT VOLTAGE

\[ V_M = \text{"MIDPOINT VOLTAGE" (A.K.A. "TRIP POINT")} \]

= POINT WHERE VTC INSECTS WITH LINE DEFINED BY VOUT = VIN

\[ \rightarrow V_M \text{ IS IN THE TRANSITION REGION, AND THEREFORE IS NOT A VALID LOGIC LEVEL} \]

\[ \rightarrow \text{ BUT, } V_M \text{ DEFINES THE "CENTER POINT" FOR VIN, WHERE:} \]

\[ \text{VIN} < V_M \Rightarrow \text{VIN IS ON "0" SIDE} \]
\[ \text{VIN} > V_M \Rightarrow \text{VIN IS ON "1" SIDE} \]

TO FIND VM, SET:

\[ \text{VIN} = VOUT = V_M \]
\[ I_{DP} = I_{DN} \]

**Figure 7.4** Inverter voltages for \( V_M \) calculation

**But, before we can use \( I_D \) equations we need to determine if FETs are saturated or triode**

**For NMOS:**

\[ V_{DS} = V_M \]
\[ V_{GS} = V_M \]

\[ \Rightarrow V_{DS} \geq V_{GS} - V_T \]
\[ V_M \geq V_M - V_T \]
\[ \checkmark \text{ Yes! (V_T > 0)} \]

\[ \Rightarrow \text{NMOS IS SATURATED} \]

**For PMOS:**

\[ |V_{DS}| = V_{DD} - V_M \]
\[ |V_{GS}| = V_{DD} - V_M \]

\[ \Rightarrow |V_{DS}| \geq |V_{GS}| - |V_T| \]

\[ \text{YES!} \]

\[ \Rightarrow \text{PMOS IS SATURATED} \]

(Note: Using magnitudes for PMOS avoids sign errors!)
CALCULATION OF MIDPOINT VOLTAGE (CONT.)

USING EQUATION IN SATURATION \Rightarrow SET \, I_{DM} = I_{DP}:

\[ \frac{B_N}{2} (V_{GSN} - V_{TN})^2 = \frac{B_P}{2} (1V_{GSP} - 1V_{TP})^2 \]

\[ \frac{B_N}{2} (V_M - V_{TN})^2 = \frac{B_P}{2} (V_{DP} - V_M - 1V_{TP})^2 \]

\[ \Rightarrow \sqrt{\frac{B_N}{B_P}} (V_M - V_{TN}) = (V_{DP} - V_M - 1V_{TP}) \]

OR

\[ V_M (1 + \sqrt{\frac{B_N}{B_P}}) = V_{DP} - 1V_{TP} + V_{TN} \sqrt{\frac{B_N}{B_P}} \]

\[ \Rightarrow V_M = \frac{V_{DP} - 1V_{TP} + V_{TN} \sqrt{\frac{B_N}{B_P}}}{1 + \sqrt{\frac{B_N}{B_P}}} \]

**NOW, THIS SHOWS THAT THE INVERTER TRIP POINT IS SET BY:**

1) \( V_{TN}, 1V_{TP} \) \( \Rightarrow \) SET BY PROCESS

2) RATIO OF \( B_N \) TO \( B_P \) \( \Rightarrow \) CONTROLLED BY DESIGNER

LOOK AT \( \frac{B_N}{B_P} \):

\[ \frac{B_N}{B_P} = (\frac{L_N}{L_P}) \left( \frac{W}{L} \right)_N \]

SET BY PROCESS

\[ \left( \frac{W}{L} \right)_P \]

SET BY DESIGNER

NOTE: \( \frac{L_N}{L_P} = \frac{m_N \cdot COX}{m_P \cdot COX} = \frac{m_N}{m_P} = \text{RATIO OF MOBILITIES OF ELECTRONS TO HOLEs} \)

TYPICALLY, \( \frac{m_N}{m_P} \approx 2 - 3 \)
Calculation of Midpoint Voltage (cont.)

Now, suppose we want to adjust $B_N, B_P$ to set $V_m$?

⇒ Re-arrange previous equation for $V_m$:

$$\sqrt{\frac{B_N}{B_P}} = \frac{V_{DD} - V_m - I_{VTP}}{V_m - V_{TN}}$$

To build a "Symmetric Inverter" with equal "0" and "1" Vin ranges ⇒

$$V_m = \frac{1}{2} V_{DD}$$

⇒ $\sqrt{\frac{B_N}{B_P}} = \frac{V_{DD} - I_{VTP}}{V_{DD} - V_{TN}}$

⇒ If: $V_{TN} \approx I_{VTP}$ (often true)

Then: $\sqrt{\frac{B_N}{B_P}} = 1$

Or, $B_N = B_P$

And since: $\frac{B_N}{B_P} = \left(\frac{W}{L}\right)_N \left(\frac{W}{L}\right)_P = 1$

⇒ Set: $\frac{\left(\frac{W}{L}\right)_N}{\left(\frac{W}{L}\right)_P} = \frac{B_P}{B_N} = \frac{M_P}{M_N} \approx \frac{1}{3}$

⇒ Make PMOS bigger than NMOS by the ratio of mobilities $\approx 2-3$!
Example 7.1
Consider a CMOS process with the following parameters

\[ k_n' = 140 \ \mu A/V^2 \quad V_{Tn} = +0.70 \ \text{V} \]
\[ k_p' = 60 \ \mu A/V^2 \quad V_{Tp} = -0.70 \ \text{V} \]  \hspace{1cm} (7.21)

with \( V_{DD} = 3.0 \ \text{V} \).

Consider the case where \( \beta_n = \beta_p \). We can verify that this is a symmetrical design by calculating

\[ V_M = \frac{3 - 0.7 + \sqrt{1(0.7)}}{1 + \sqrt{1}} = 1.5 \ \text{V} \]  \hspace{1cm} (7.22)

so that \( V_M \) is one-half the value of the power supply voltage. To achieve this design, we must choose the device aspect ratios such that

\[ \frac{\beta_p}{\beta_n} = \frac{k_p'}{k_n'} \left( \frac{W}{L} \right)_n = 1 \]  \hspace{1cm} (7.23)

where we recall that the process transconductance parameters \( k' \) are given by \( k' = k_n'C_{ov} \) and are set by the processing. For the present case, we rearrange the expression to read

\[ \left( \frac{W}{L} \right)_p = \left( \frac{W}{L} \right)_n \left( \frac{k_n'}{k_p'} \right) \]  \hspace{1cm} (7.24)

so that

\[ \left( \frac{W}{L} \right)_p = \left( \frac{140}{60} \right) \left( \frac{W}{L} \right)_n = 2.33 \left( \frac{W}{L} \right)_n \]  \hspace{1cm} (7.25)

This shows that the pFET must be about 2.33 times larger than the nFET.

Let us now examine the case where the nFET and the pFET have the same aspect ratio: \( (W/L)_n = (W/L)_p \). With the values provided in the problem statement,

\[ \frac{\beta_n}{\beta_p} = \frac{k_n'}{k_p'} = 2.33 \]  \hspace{1cm} (7.26)

so that the midpoint voltage is given by

\[ V_M = \frac{3 - 0.7 + \sqrt{2.33 \times (0.7)}}{1 + \sqrt{2.33}} = 1.33 \ \text{V} \]  \hspace{1cm} (7.27)

This choice shifts \( V_M \) to a value that is smaller than \( (V_{DD}/2) \).
Now, to build a symmetric inverter VTC requires:

$$\left( \frac{W}{L} \right)_P = \left( \frac{W}{L} \right)_N \left( \frac{\mu_N}{\mu_P} \right) \approx 2-3 \times \left( \frac{W}{L} \right)_N$$

Is this worth the cost in silicon area?

\[ \text{Most VLSI digital cell libraries use } \left( \frac{W}{L} \right)_P = \left( \frac{W}{L} \right)_N \text{ to save silicon area!} \]

\[ \text{Having a symmetric curve is not critical to } \text{digital circuits!} \]
SWITCHING CHARACTERISTICS OF CMOS INVERTERS

![Switching Waveform Diagram]

**Figure 7.7** General switching waveforms

- $t_R$ = "Rise Time"
- $t_F$ = "Fall Time"

Now, we can model these as R-C responses!

![R-C Circuit Diagrams]

**Time Constants:**

$$
\begin{align*}
\tau &= R_p C_{out} \\
\text{where:} & \quad \frac{1}{R_p} = \frac{1}{\beta_p (V_{pp} - V_{th})} \\
\tau &= R_n C_{out} \\
\text{where:} & \quad \frac{1}{R_n} = \frac{1}{\beta_n (V_{pp} - V_{th})}
\end{align*}
$$

**Note:** This assumes both FETs operate in *triode*.

→ True for most of the transient step, but not all!

E.g., if $V_{in}$ steps from 0 to $V_{pp}$ at $t = 0^+$, →

$V_{DSS} = V_{GSN} = V_{pp}$ at $t = 0^+ →$ saturated, but,

as soon as $V_{out}$ drops to $V_{pp} - V_{in} →$ triode (most of the transient)
Figure 7.8 RC switch model equivalent for the CMOS inverter

Figure 7.10 Evolution of the inverter switching model

$\text{TOTAL CAPACITIVE LOAD} = C_{\text{OUT}} = C_L + C_{PP} + C_{PN}$

Now, how to calculate the parasitic caps?
CALCULATION OF MOS CAPACITANCES

FIRST, LOOK AT GATE CAP!

![Diagram of gate capacitance in a FET](image)

**Figure 6.21** Gate capacitance in a FET

![Diagram of gate-source and gate-drain capacitance](image)

**Figure 6.22** Gate-source and gate-drain capacitance

\[ C_{\text{GATE}} = W \cdot L \cdot C_{\text{OX}} \] (TOTAL)

AND, IN TRIODE:

\[ C_{GS} = C_{GD} = \frac{1}{2} W \cdot L \cdot C_{\text{OX}} \]
Next, look at PN junction caps!

Figure 6.23 Junction capacitances in a MOSFET

Now, to find $C_{SB}$ and $C_{DB}$, must consider both the area and sidewall contributions:

![Diagram of MOSFET with capacitance annotations]

Figure 6.25 Calculation of the FET junction capacitance

Area of $C_{bottom} = A_{bot} = x \cdot w$

Area of $C_{sidewall} = A_{sw} = 2(w \cdot x_j) + 2(x \cdot x_j)$

$A_{sw} = (2w + 2x) \cdot x_j$

"Perimeter" = $2w + 2x$

Note: Sidewall cap is usually given as "capacitance per unit perimeter"
RECALL FOR A PN JUNCTION CAP!

\[ C = \frac{C_0}{1 + \left( \frac{V_R}{\Phi_0} \right)^{M_j}} \]

WHERE:

\[ \Phi_0 = \frac{kT}{q} \ln \left( \frac{N_A N_D}{m^2} \right) \]

\[ C_0 = \text{ZERO BIAS CAPACITANCE} \]
\[ V_R = \text{REVERSE BIAS ACROSS JUNCTION} \]
\[ \Phi_0 = \text{"BUILT-IN" JUNCTION VOLTAGE} \]
\[ M_j = \text{"GRADING COEFFICIENT"} \]

AND, \[ C_0 = C_j A \]

\[ C_j = \text{JUNCTION CAP PER UNIT AREA} \]
\[ A = \text{AREA OF JUNCTION} \]

**Figure 6.24** Junction capacitance variation with reverse voltage

- \( M_j \) IS USUALLY \( \approx \frac{1}{2} \) FOR AREA CAP (STEP JUNCTION)
- \( M_j \) IS USUALLY \( \approx \frac{1}{3} \) FOR SIDEWALL CAP (LINEAR JUNCTION)

*OFTEN USE \( C_0 \) VALUE (VALUE FOR \( V_R = \Phi_0 = M_{\text{MAX}} \)) IN CALCULATIONS AS "WORST-CASE" VALUE*
$P_{SW} = 2(W+x) = \text{PERIMETER OF JUNCTION}$

$C_{SW} = C_{jsw} P_{SW} = \text{CAPACITANCE OF JUNCTION SIDEWALL}$

WHERE:

$C_{jsw} = C_{jx} F_{om} = \text{SIDEWALL CAPACITANCE PER UNIT PERIMETER}$

**TOTAL JUNCTION CAP:**

$C_{total} = C_{Bot} + C_{SW}$

$= C_{j} A_{Bot} + C_{jsw} P_{sw}$

$C_{total} = C_{j} (WX) + C_{jsw} (2W + 2x)$

OR, INCLUDING VOLTAGE DEPENDANCE:

$C_{\text{total}} = \frac{C_{j} A_{Bot}}{(1 + \frac{V}{V_{th}})^{M_j}} + \frac{C_{jsw} P_{sw}}{(1 + \frac{V}{V_{th_{sw}}})^{M_{jsw}}}$

**NOTE:** $\phi_0, M_j$ USUALLY DIFFERENT FOR AREA & SIDEWALL

---

**Figure 6.27** Final construction of the nFET RC model

- $C_{Dn} = C_{GSS} + C_{GBn} = \frac{1}{2} C_{ox} L \omega_n + C_{jnp} A_n + C_{jswp} P_n$

- $C_{Dp} = C_{GSS} + C_{DBn} = \frac{1}{2} C_{ox} L \omega_p + C_{jgp} A_p + C_{jswp} P_p$
Example 7.2
Let us apply this analysis to find the capacitances in the NOT gate shown in Figure 7.11. It is assumed that all dimensions have units of microns (μm).

First we will find the gate capacitances using

\[ C_{DP} = (2.70)(1)/8 = 21.6 \text{ fF} \]  
\[ C_{DN} = (2.70)(1)/4 = 10.8 \text{ fF} \]  

(7.34)

Next, note that the overlap distance \( L_o \) is specified as 0.1 μm, which should be included in the area and perimeter factors in the junction capacitances. For the pFET, the p+ capacitance is

\[ C_P = C_{Pdot} + C_{JINF}P_{INF} \]  

(7.35)

**Figure 7.11** Example of capacitance calculations

so

\[ C_P = (1.05)(8)(2.1) + (0.32)(8 + 2.1) = 24.10 \text{ fF} \]  

(7.36)

The total capacitance at the pFET drain is therefore given by

\[ C_{DP} = \frac{21.6}{2} + 24.10 = 34.9 \text{ fF} \]  

(7.37)

The nFET drain is analyzed using the same approach. The n+ junction capacitance is

\[ C_n = (0.86)(4)(2.1) + (0.24)(4)(4 + 2.1) = 10.15 \text{ fF} \]  

(7.38)

so that

\[ C_{DN} = \frac{10.8}{2} + 10.15 = 15.55 \text{ fF} \]  

(7.39)

is the total capacitance at the drain of the nFET. Adding gives

\[ C_{FET} = C_{DP} + C_{DN} \]  

\[ = 34.9 + 15.55 \]  

\[ = 50.45 \text{ fF} \]  

(7.40)

as the total internal FET capacitance. The total capacitance at the output is

\[ C_{out} = 50.45 + C_L \]  

(7.41)

in fF, where \( C_L \) is the external load (also in fF).
FALL TIME CALCULATION

Figure 7.12 Discharge circuit for the fall time calculation

- LOOKS LIKE A 1ST ORDER R-C CIRCUIT!
  \[ V_{out}(t) = V_{DD} e^{-t/T_N} \]
  \[ \text{WHERE: } T_N = R_N \cdot C_{OUT}, \quad R_N = \frac{1}{B_N \cdot (V_{DD} - V_N)} \]

NOW, USUALLY DEFINE \( t_F = "FALL \ TIME" \ AS THE \ TIME \ REQUIRED \ TO \ GO \ FROM \ 90\% \ TO \ 10\% \)

\[ \Rightarrow \text{REARRANGE EQUATION: } \quad t = T_N \ln \left( \frac{V_{DD}}{V_{OUT}} \right) \]

\[ \Rightarrow t_F = t_Y - t_X \]

\[ t_F = T_N \ln \left( \frac{V_{DD}}{0.9 \cdot V_{PP}} \right) - T_N \ln \left( \frac{V_{DD}}{0.1 \cdot V_{PP}} \right) \]

\[ t_F = T_N \ln(9) \approx 2.2 \cdot T_N = "FALL \ TIME" \]

ALSO KNOWN AS \( t_{HL} = "HIGH-TO-LOW" \ TIME \)

(SOMETIMES ALSO LOOK AT 20-80\% FALL TIME)
RISE TIME CALCULATION

- LOOKS LIKE A 1ST ORDER R-C CIRCUIT!

⇒ \( V_{\text{OUT}}(t) = V_{\text{DD}} \left( 1 - e^{-t/T_p} \right) \)

WHERE: \( T_p = R_P C_{\text{OUT}} \), \( R_P = \frac{V_P}{V_{\text{DD}} - 1.4 V_T} \)

OR, SOLVING FOR \( t \) ⇒ \( t = T_p \ln \left( \frac{V_{\text{DD}}}{V_{\text{DD}} - V_{\text{OUT}}} \right) \)

AND, SOLVING FOR THE 10-90% RISE TIME:

\( t_R = t_{90} - t_{10} = T_p \ln \left( \frac{V_{\text{DD}}}{V_{\text{DD}} - 0.9 V_{\text{DD}}} \right) - T_p \ln \left( \frac{V_{\text{DD}}}{V_{\text{DD}} - 0.1 V_{\text{DD}}} \right) \)

\( = T_p \ln \left( \frac{1}{9} \right) - T_p \ln \left( \frac{1}{10} \right) \)

\( = T_p \ln \left( \frac{9}{10} \right) = T_p \ln (9) \)

\( t_R = T_p \ln (9) \approx 2.2 T_p = \text{"RISE TIME"} \)

ALSO KNOWN AS \( t_{\text{HL}} = \text{"LOW-TO-HIGH" TIME} \)

* NOTE SIMILARITY TO FALL TIME!

AND, \( f_{\text{MAX}} = \frac{1}{t_{\text{HL}} + t_{\text{GH}}} = \text{"MAXIMUM SIGNAL FREQUENCY"} \)

\( \rightarrow \text{MAX FREQ FOR 101010... PATTERN} \)
Example 7.3
Consider an inverter circuit that has FET aspect ratios of \((W/L)_n = 6\) and \((W/L)_p = 8\) in a process where

\[
k_n = 150 \ \text{µA/V}^2 \quad V_{TN} = +0.70 \ \text{V} \\
k_p = 62 \ \text{µA/V}^2 \quad V_{TP} = -0.85 \ \text{V}
\]

and uses a power supply voltage of \(V_{DD} = 3.3 \ \text{V}\). The total output capacitance is estimated to be \(C_{out} = 150 \ \text{fF}\). Let us compute the rise and fall times using the equations derived above.

Consider first the fall time. The pFET resistance is given by

\[
R_p = \frac{1}{\beta_p(V_{DD} - |V_{TP}|)} = \frac{1}{(62 \times 10^6)(3.3 - 0.85)} = 822.9 \ \Omega
\]

The time constant for the charging event is computed using the RC product \(R_p C_{out}\) to find

\[
\tau_p = (822.9)(150 \times 10^{-15}) = 123.43 \ \text{ps}
\]

where 1 ps (picosecond) is \(10^{-12}\) sec. The rise time is

\[
t_r = 2.2 \tau_p = 271.55 \ \text{ps}
\]

The fall time is calculated in a similar manner. First, we find the nFET resistance

\[
R_n = \frac{1}{\beta_n(V_{DD} - V_{TN})} = \frac{1}{(150 \times 10^5)(3.3 - 0.70)} = 427.35 \ \Omega
\]

so that the discharge time constant is

\[
\tau_n = (427.35)(150 \times 10^{-15}) = 64.1 \ \text{ps}
\]

The fall time is

\[
t_f = 2.2 \tau_n = 141.0 \ \text{ps}
\]

Combining these results, the maximum signal frequency is

\[
f_{\text{max}} = \frac{1}{t_r + t_f} = \frac{1}{(271.55 + 141.0) \times 10^{-12}} = 2.42 \ \text{GHz}
\]

where 1 GHz = \(10^9\) Hz. Although this is a very high frequency, it is important to remember that this refers only to a single inverter.
Propagation Delay

- Estimate of delay time from input to output
- Measured to 50% points

![Figure 7.14 Propagation time definitions](image)

Using the previous equations for $V_{out}(t)$ as $V_{out}$ goes from $V_{DD}$ to $V_{DD}/2$ and from 0 to $V_{DD}/2$

$$x_{PF} = \ln(2) \gamma_N \approx 0.7 \gamma_N$$
$$x_{PR} = \ln(2) \gamma_P \approx 0.7 \gamma_P$$

AND,

$$x_P = \frac{(x_{PF} + x_{PR})}{2} \approx 0.35 (\gamma_N + \gamma_P)$$

Note: $x_P$ = "Propagation Delay" is a useful "Figure of Merit" for a logic family.
**Fan-out and Loading**

![Diagram](image)

**Figure 7.9** Input capacitance and load effects

- "Fan-out" refers to how many identical gates a given logic gate drives.

![Graph](image)

**Figure 7.15** General behavior of the rise and fall times

\[ t_R \approx 2.2 \, R_p \, (C_{FET} + C_L) \]
\[ t_F \approx 2.2 \, R_N \, (C_{FET} + C_L) \]

\[ \Rightarrow t_R = t_{R_0} + \alpha_p C_L \]
\[ t_F = t_{F_0} + \alpha_N C_L \]

Where:
- \( C_{FET} = \) Parasitics of logic gate
- \( C_L = \) External load

\[ t_{R_0} = 2.2 \, R_p \, C_{FET} \] "Self delay" of logic gate (delay with \( C_L = 0 \))
\[ t_{F_0} = 2.2 \, R_N \, C_{FET} \]
\[ \alpha_p = 2.2 \, R_p \] Slope of line as \( C_L \) increases
\[ \alpha_N = 2.2 \, R_N \] (Speed vs Area tradeoff!)
Example 7.4
Let us use the results of Example 7.3 to find the general delay equations for the case where the internal FET capacitance is $C_{FET} = 80$ fF.

The rise time $t_r$ is controlled by the pFET that has a resistance of $R_p = 822.9$ Ω. The slope is given by

$$\alpha_p = 2.2R_p = 1.810.4\Omega$$  \hspace{1cm} (7.74)

while

$$t_{r0} = 2.2R_pC_{FET}$$
$$= 2.2(822.9)(80 \times 10^{-15})$$
$$= 144.9 \text{ ps}$$ \hspace{1cm} (7.75)

The rise time can thus be written in the form

$$t_r = t_{r0} + \alpha_p C_L$$
$$= 144.9 + 1.810C_L \text{ ps}$$ \hspace{1cm} (7.76)

which requires that $C_L$ be in units of fF.

For the fall time equation, we calculate

$$\alpha_n = 2.2(427.35) = 940.2\Omega$$ \hspace{1cm} (7.77)

and

$$t_{f0} = 2.2(940.2)(80 \times 10^{-15}) = 165.5 \text{ ps}$$ \hspace{1cm} (7.78)

yielding

$$t_f = 165.5 + 0.940C_L \text{ ps}$$ \hspace{1cm} (7.79)

as the general expression.

As an example of using these equations, suppose that the load is specified as $C_L = 150$ fF. We compute

$$t_r = 144.9 + 1.810(150) = 416.4 \text{ ps}$$
$$t_f = 165.5 + 0.940(150) = 306.5 \text{ ps}$$ \hspace{1cm} (7.80)

for the rise and fall times at the output. This corresponds to a maximum switching frequency for the gate of $f_{max} = 1.38 \text{ GHz}$. 


**Power Dissipation**

![Diagrams showing VTC and DC current flow](image)

**Figure 7.17** DC current flow

\[ P_{total} = V_{DD} I_{DDQ} \] but \( I_{DD} \neq \text{constant!} \)

\[ P_{total} = P_{DC} + P_{dynamic} \]

\[ P_{DC} = V_{DD} I_{DDQ} \approx \text{small (usually!)} \]

**Dynamic Power:**

![Diagram showing input voltage, charge, and discharge](image)

**Figure 7.18** Circuit for finding the transient power dissipation

- \( C_{out} \) is 1st charged to \( V_{DD} \), then discharged to GND

\[ I_{avg} = \frac{Q}{T} = \frac{C_{out} V_{DD}}{T} \]

\[ P_{avg} = V_{DD} I_{avg} = C_{out} V_{DD}^2 f \]  

\[ P_{total} = C_{out} V_{DD}^2 f + V_{DD} I_{DDQ} \]

**Note:** This neglects "shoot-through" current!

(Note from Fig. 7.10(c)), lots of I flows when both FETs are ON.

- Power can go down if not switched every CLK = "activity factor".
DC CHARACTERISTICS OF CMOS NAND GATES

Figure 7.19 NAND2 logic circuit

Figure 7.24 Simplified $V_M$ circuit for the NAND2 gate

Figure 7.20 NAND2 VTC analysis

- FOR SIMULTANEOUS SWITCHING, THE NAND2 GATE LOOKS LIKE AN INVERTER WITH 2 N-FETS IN SERIES AND 2 P-FETS IN PARALLEL $\Rightarrow$ SHIFTS VTC TO RIGHT!

$\Rightarrow$ THINK OF IT LIKE 2 RESISTORS IN PARALLEL (PMOS) AND 2 RESISTORS IN SERIES (NMOS). THEN, WHAT $V_{IN}$ IS NEEDED TO MAKE $2R_N = \frac{1}{2}R_P$?

$V_M = \frac{V_{DD} - |V_{TP}| + \frac{1}{2} \frac{\beta_n}{\beta_p} V_{TH}}{1 + \frac{1}{2} \frac{\beta_n}{\beta_p}}$

$V_M = \frac{V_{DD} - |V_{TP}| + \frac{1}{N^4} \frac{\beta_n}{\beta_p} V_{TM}}{1 + \frac{1}{N^4} \frac{\beta_n}{\beta_p}}$

2-INPUT NAND

$N$-INPUT NAND

NOTE: CAN ALSO SCALE $R_N, R_P$.
Another way to look at it!

Figure 7.21 Layout of NAND2 for \( V_M \) calculation

2 series NMOS FETs look like a single FET with \( 2 \times L \)

\[ \Rightarrow \beta_{N(\text{eq})} = \frac{\beta_N}{2} \]

2 parallel PMOS FETs look like a single FET with \( 2 \times W \)

\[ \Rightarrow \beta_{P(\text{eq})} = 2 \beta_P \]
DC CHARACTERISTICS OF CMOS NOR GATES

Figure 7.25: NOR2 circuit

Figure 7.27: NOR2 $V_M$ calculation for simultaneous switching

Figure 7.26: NOR2 VTC construction

- VERY SIMILAR TO NAND2 CASE!
- FOR SIMULTANEOUS SWITCHING, THE NOR2 GATE LOOKS LIKE AN INVERTER WITH 2 N-FETS IN PARALLEL AND 2 P-FETS IN SERIES => SHIFTS VTC TO LEFT!
- WHAT $V_{IN}$ IS NEEDED TO MAKE $V_M = \frac{1}{2} R_N = 2R_P$?

$V_M = \frac{V_{DD} - |V_{TH}| + 2 \frac{\beta_n}{\beta_p} V_{TH}}{1 + 2 \frac{\beta_n}{\beta_p}}$

$V_M = \frac{V_{DD} - |V_{TH}| + N \frac{\beta_n}{\beta_p} V_{TH}}{1 + N \frac{\beta_n}{\beta_p}}$

2-INPUT NOR

N-INPUT NOR

NOTE: CAN ALSO SCALE $R_N, R_P$. 
SWITCHING CHARACTERISTICS OF CMOS NAND GATES

- **CONSIDER "WORST-CASE" RISE/FALL TIMES**
- **NOTE INCREASE IN COUT DUE TO PARALLEL P-FETS**
- **FOR RISE TIME, LOOKS LIKE AN INVERTER!**
  \[ t_R \approx 2.2 \tau_p \]
  
  **WHERE:**
  \[ \tau_p = R_p \cdot C_{out} \]
  
  (2X THIS SPEED WITH BOTH PMOS ON!)

FOR FALL TIMES:
- **COUT DISCHARGES THROUGH 2RN, BUT ALSO MUST DISCHARGE Cx!**
  
  \[ t_f = \tau_N + \tau_N' \]

  \[ \tau_N = 2R_N \cdot C_{out} + R_N \cdot C_x \]  

  **(BY SUPERPOSITION)  \( \text{"EMLMORE FORMULA"} \)**

  AND:  \[ t_f = 2.2 \tau_N \]

  \[ t_f > t_R \]

  **NOW, CAN EQUALIZE \( t_f \) AND \( t_R \) BY SIZING UP N-FETS!**

  \[ W/ \text{Cx, WOULD MAKE } R_N = \frac{1}{2} R_p \quad (\text{OR } 1/3 \text{ FOR 3-INPUT NAND}) \]

  WITH Cx, NEED TO MAKE R_N LARGER
SWITCHING CHARACTERISTICS OF CMOS NOR GATES

**Figure 7.30** NOR2 circuit for switching time calculations

- Consider "worst-case" rise/fall times
- Note increase in C_out due to parallel N-FETs

**Figure 7.31** Subcircuits for the NOR2 transient calculations

For rise times:
- C_out charges through 2R_P, C_y charges through R_P

\[ \gamma_p = \gamma_{p1} + \gamma_{p2} \]

\[ \gamma_p = 2R_PC_{out} + R_PC_y \]

AND: \[ k_R = 2, 2, \gamma_p \rightarrow k_R > k_F \]

- Once again, we can equalize \( k_R, k_F \) by sizing up PMOS
- To make an NOR gate as fast as a NAND gate!

\[ \Rightarrow \text{lots of silicon area, since } R_P > R_N \text{ for same } V \]

\[ \Rightarrow \text{due to } n_N \approx 2-3 \times n_P ! \]
SWITCHING CHARACTERISTICS OF COMPLEX GATES

EXAMPLE:

\[ F = x \cdot (y + z) \]

\[ \text{Assume:} \]
1) ALL PMOS \( W/L \) \& EQUAL
2) ALL NMOS \( W/L \) \& EQUAL

\[ \text{Figure 7.32 Complex logic gate circuit.} \]

*LOOK FOR WORST-CASE CHARGE/DISCHARGE PATHS!*

- FOR \( t_F \), WORST-CASE WHEN \( x = 1 \) AND \( y \) OR \( z = 1 \)
  \[ \Rightarrow 2 \text{ SERIES NMOS FETS (LIKE 2-INPUT NAND)} \]
  \[ \Rightarrow t_F = 2.2 T_n = 2.2 \left[ 2 R_{CN} + R_N C_n \right] \]

- FOR \( t_R \), WORST-CASE WHEN \( x = 1, y = \phi, z = \phi \)
  \[ \Rightarrow 2 \text{ SERIES PMOS FETS (LIKE 2-INPUT NOR)} \]
  \[ \Rightarrow t_R = 2.2 T_p = 2.2 \left[ 2 R_P + R_C C_P \right] \]

*CAN BE VERY SLOW AS:*

1) \# OF SERIES FETS GOES UP, AND/OR,
2) \# OF PARALLEL FETS GOES UP (\( C_{OUT} \uparrow \), OR \( C_N, C_P \uparrow \))
SIZING GATES FOR TRANSIENT PERFORMANCE

Figure 7.34 Relative FET sizing

(a) Inverter
(b) NAND2
(c) NOR2

\[ \beta_p = \text{INVERTER} \]
\[ \beta_n = \text{VALUE FOR LOGIC GATE} \]

\text{(SYNTAX USED HERE)}

Figure 7.35 Sizing for 3-input gates

(a) NAND3
(b) NOR3

\[ \beta_p = 2\beta_p \]
\[ \beta_n = 3\beta_n \]

\text{EQUALIZES WORST-CASE DELAYS TO 1ST ORDER ONLY!}

\text{BEST-CASE CAN BE MUCH FASTER!}

\text{ALSO CORRECTS FOR TRIP-POINT} (V_m)

Figure 7.36 Sizing of a complex logic gate