MOS Basics, Structures and Layouts

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Outline

• Semiconductor basics, PN junctions
• MOSFET basics
  – Device structure
  – Gate capacitance
  – MOSFETs as switches
• CMOS layers & MOS structures
• Typical layouts
  – Inverters (NOT gates), NANDs, NORs
  – Complex gates, AOI
  – Stick diagrams
\( p = n = n_i \) intrinsic carrier concentration in equilibrium
\( n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \) at room temperature (27°C = 300K)

\( p n = n_i^2 \) mass-action law

\( \sigma = q(\mu_p p + \mu_n n) \) semiconductor conductivity

where: \( q = \text{electronic charge} = 1.6 \times 10^{-19} \)

\( \mu_p, \mu_n \) are the mobilities of holes & electrons
Example 3.1
Suppose that the donor doping density is \( N_d = 2 \times 10^{17} \) cm\(^{-3} \). The electron density is

\[
n_n \approx N_d = 2 \times 10^{17} \text{ cm}^{-3}
\]  \hspace{1cm} (3.21)

while the hole concentration is

\[
p_n \approx \frac{n_i^2}{N_d} = \frac{(1.45 \times 10^{10})^2}{2 \times 10^{17}}
\]  \hspace{1cm} (3.22)

which gives

\[
p_n \approx 1 \times 10^3 \text{ cm}^{-3}
\]  \hspace{1cm} (3.23)

Obviously, \( n_n \gg p_p \) holds for the sample.
Example 3.2
Consider a sample of silicon that is doped p-type with boron added at a density of \(10^{15}\) cm\(^{-3}\). The majority charge carriers are holes with a density of

\[
    p_p = 10^{15} \text{ cm}^{-3}
\]  

(3.29)

while the minority carrier electron density is

\[
    n_p = \frac{(1.45 \times 10^{10})^2}{10^{15}} = 2.2 \times 10^5 \text{ cm}^{-3}
\]  

(3.30)

For this sample, the mobilities are given by \(\mu_n = 1350 \text{ cm}^2/\text{V-sec}\) and \(\mu_p = 450 \text{ cm}^2/\text{V-sec}\). The conductivity is

\[
    \sigma = (1.6 \times 10^{-19})[(1350)(2.2 \times 10^5) + (450)(10^{15})]
\]  

\[
    = 0.072 \quad [\Omega\text{-cm}]^{-1}
\]  

(3.31)

which is equivalent to a resistivity of

\[
    \rho = \frac{1}{0.08} = 13.9[\Omega\text{-cm}]
\]  

(3.32)

A quick check on the values shows that \(\mu_p p_p \gg \mu_n n_p\) for this example. In general, the resistivity of silicon samples is on the order of 1 to 10 \(\Omega\)-cm.
Figure 3.15 Formation and characteristics of a pn junction
Figure 3.12 Layers used to create a MOSFET
Figure 3.13  Views of a MOSFET
\[ C = \frac{\varepsilon}{t_{\text{ins}}} \]

where: \( \varepsilon = \text{insulator permitivity} \)
\( t_{\text{ins}} = \text{insulator thickness} \)
Figure 3.18 The gate capacitance in an n-channel MOSFET
Figure 3.19 Controlling current flow in an nFET
Figure 3.20 Switching behavior of a pFET
Figure 3.23 MOSFET layers in an n-well process

From this drawing, we can identify the following layer types:

- p-substrate
- n-well
- n+ (nFET drain/source)
- p+ (pFET drain/source)
- gate oxide
- gate (polysilicon)
Figure 3.24  Top view FET patterning
Figure 3.25  Metal interconnect layers
Figure 3.26  Interconnect layout example
Figure 3.27 Silicon patterning for two series-connected nFETs
Figure 3.28 Three series-connected nFETs
Figure 3.29 Parallel-connected FET patterning

Figure 3.30 Alternate layout strategy for parallel FETs
Figure 3.31 Translating a NOT gate circuit to silicon
Figure 3.32 Alternate layout for a NOT gate
Figure 3.33  Two NOT gates that share power supply and ground
Figure 3.34 Non-inverting buffer

(a) Logic diagram

(b) Layout
Figure 3.35 Layout of a transmission gate with a driver
Figure 3.36 NAND2 layout

(a) Circuit

(b) Layer design
Figure 3.37 NOR2 gate design
Figure 3.38 NAND2-NOR2 layout comparison
Figure 3.39 Layout for 3-input gates.
Figure 3.40 Extension of layout technique to a complex logic gate
Figure 3.41 Creation of the dual network
Figure 3.42 A general 4-input AOI gate
Figure 3.43 General gate layout geometry
Figure 3.44 Basic stick layout diagram