Testing of VLSI Chips

1. After a silicon wafer is processed through the fabrication line, it must be tested to determine:
   1) If the processing steps were performed correctly, resulting in good FETs, vias, metal lines, etc.
   2) Which chips, or "die", contain process defects
   3) Which chips are grossly functional
   4) Which chips meet all specifications

2. All wafers are 1st tested to make sure a good process lot was obtained:
   → Several sites on the wafer are dedicated to "prop-ins", or "wat keys" (WAT = "Wafer Acceptance Test")
   → Each of these test sites contain sample PMOS and NMOS FETs of various sizes, as well as special test structures to check for bad metal, vias, contacts, etc.
   → The prop-ins are often built into the "scribe lines" between adjacent chips
   → Various electrical parameters are measured, such as MOSFET Vt, IDSAT, etc.
      (IDSAT = Ip with VDS = VGS = VDD)
   → Once a good process lot has been verified, the wafer is released for further testing
• AFTER A GOOD PROCESS HAS BEEN VERIFIED, EACH INDIVIDUAL CHIP MUST BE CHECKED!

→ A “TEST PROBE” IS USED TO MAKE CONTACT TO EACH CHIP, ONE AT A TIME

→ A FEW SIMPLE ELECTRICAL TESTS ARE RUN, (MOSTLY DC OR LOW SPEED SIGNALS) TO CHECK FOR GROSS DEFECTS (E.G., PROCESS DEFECT)

→ BAD DIE ARE MARKED WITH AN INK POT ("INKED")

→ SOMETIMES SIMPLE TRIMS ARE PERFORMED DURING WAFER SORT (E.G., BANDCAP TRIMS)

• AFTER BAD CHIPS HAVE BEEN IDENTIFIED AT PROBE, THE WAFER IS “SCRIBE” OR “SAWED” INTO INDIVIDUAL DIE, AND THE GOOD CHIPS SEPARATED FOR FURTHER TESTING

• SOMETIMES A “WAFER MAP” IS CREATED, SHOWING THE LOCATIONS OF ALL BAD DIE, OR EVEN UNIQUELY IDENTIFYING ALL DIE

→ CAN ASSIST IN DEBUG
CHIP TESTING

- After wafer sort, the resulting good chips are packaged.
- The packaged chips are then tested to see if they meet all specifications using high-speed "ATE" (Automatic Test Equipment).
  - A key part of the cost of a chip is the test cost.
  - Lots of effort often goes into reducing test time to reduce cost.
- "Test vectors" are input to the chip, and the outputs are checked to verify that the chip is functional and meets all specifications.
  - "Test vectors" are arrays of binary inputs.
  - "Test vector generation" is the task of creating a set of vectors to check the operation of the chip.
  - "Functional testing" directly checks the functions of the chip.

"Test coverage" of > 90% is desired (>70% of all gates verified good).

Figure 16.5 Overview of the testing problem.
CHIP TESTING (CONT.)

• "SCAN" IS A TEST METHODOLOGY OFTEN BUILT INTO DIGITAL CHIPS
  → ALL FLIP-FLOPS ARE PROVIDED WITH AN ALTERNATE INPUT FOR DATA (THROUGH A MIXED INPUT), AS WELL AS A SEPARATE CLOCK INPUT FOR SCAN TESTING.
  → THE FFs ARE CONNECTED TOGETHER IN ONE OR MORE "SCAN CHAINS".
  → TESTING IS DONE BY ENTERING A SPECIAL TEST MODE CALLED "SCAN MODE," WHERE A TEST VECTOR IS INPUT TO EACH SCAN CHAIN AND THE BITS CLOCKED THROUGH ALL FFs IN THE CHAIN, WITH THE RESULTING OUTPUT CHECKED FOR ERRORS.

• "BOUNDARY SCAN" (A.K.A., "JTAG") IS A SIMILAR TEST METHOD USED TO CHECK ALL INPUTS, OUTPUTS, AND PADS, WHICH ARE CONNECTED IN A CHAIN AND SCANNED FOR ERRORS DUE TO DEFECTS.

• "IPOB TESTING" IS OFTEN PERFORMED FIRST, BEFORE ALL OTHER TESTS TO SAVE TIME BY ELIMINATING GROSSLY BAD CHIPS.
  → CHECKS LEAKAGE CURRENT (NO CLOCK).
  → LESS USEFUL IN NEW PROCESSES WITH HIGH LEAKAGE.

![Image](image_url)

**Figure 16.14** Basic I/O test
Several different types of defects, or "faults" can occur.

Figure 16.6 MOSFET fault models

(a) Shorted

(b) Open

Figure 16.7 Fault model examples

(a) Gate-1 fault

(b) Gate-drain short

Figure 16.9 NAND2 gate with stuck-at faults

(a) Stuck-at-1 fault

(b) Stuck-at-0 fault
Figure 16.8 Gate-oxide short in an nFET
RELIABILITY OF CMOS CHIPS

![Bathtub reliability curve]

- **Typical chips are designed to last from 7 years - 20 years**, depending on application.
- The reliability vs time (hours) curve on a log scale follows a "bathtub curve."
  - Early failures due to "infant mortality."
  - Random failures occur throughout the lifetime of the chip.
  - Wear-out failures occur as the chips reach the end of their life.
- The "mean time to failure" is the average lifetime of a group of chips.
- Before sale, chips are typically "burned in" by operating them at high temperatures and/or supply voltages to weed out the chips subject to infant mortality.
- "Accelerated-stress life testing" is often done by testing under extreme conditions to estimate lifetimes quickly.