For each of the following questions, choose the best response. (2 points each)

1. If the length of an interconnect line is doubled, the delay through the line will:
   a) Increase by 1.5 x
   b) Increase by 2.0 x
   c) Increase by 4.0 x
   d) Increase by 8.0 x
   e) Stay the same

2. If the width of an interconnect line is doubled, the delay through the line will:
   a) Increase by > 2 x
   b) Increase by < 2 x
   c) Decrease by > 2 x
   d) Decrease by < 2 x
   e) Stay the same

3. Hold time violations can be caused by:
   a) Too many logic gates placed between registers.
   b) Large clock skews.
   c) Large flip-flop clock-to-Q delays.
   d) Large flip-flop setup times.
   e) All of the above.

4. Often the first test run on a finished chip is:
   a) IDDQ
   b) JTAG
   c) SCAN
   d) Functional
   e) None of the above

5. Which of the following advanced CMOS techniques can have errors due to erroneous evaluation?
   a) Tri-state logic.
   b) Pseudo-NMOS logic.
   c) Domino logic.
   d) Standard dynamic logic.
   e) None of the above.

6. Which of the following are a disadvantage of dynamic logic?
   a) More errors due to charge sharing than with standard CMOS logic.
   b) More errors due to crosstalk than with standard CMOS logic.
   c) More errors due to leakage than with standard CMOS logic.
   d) All of the above.
   e) None of the above.
7. In an SRAM array, a dual-core arrangement is often used to:
   a) Reduce capacitance on the word lines.
   b) Increase symmetry in the core layout.
   c) Improve the aspect ratio of the core layout.
   d) Ease routing for the column MUX’s.
   e) All of the above.

8. Types of reliability problems seen on a Bathtub curve include:
   a) Wear-out failures
   b) Random failures
   c) Infant mortality
   d) None of the above.
   e) All of the above.

9. The most popular SRAM cell uses:
   a) 1 FET
   b) 4 FETs
   c) 6 FETs
   d) 8 FETs
   e) None of the above.

10. When scaling a chain of inverters to drive a large capacitive load, the optimal scale factor is:
    a) 2.00 x
    b) 2.71 x
    c) 3.14 x
    d) 4.00 x
    e) None of the above.

For each of the following, choose either: a) True or b) False (2 points each)

11. Precharge and evaluate phases are used in ratioed logic.
12. Snap-back and field-oxide devices are often used in pads to provide ESD protection.
13. Schmitt triggers are often used in pads to protect against latch-up.
14. Ground bounce occurs when the average current through a bond wire gets too large.
15. Two major concerns in distributing power across an IC are ohmic drops and electromigration.
16. Transmission gates are seldom included in standard cell libraries due to CAD tool problems.
17. Carry look-ahead adders are both faster and smaller than ripple-carry adders.
18. Clock trees are often used to minimize skew when distributing clocks across an IC.
19. Clocked CMOS uses tri-state switches to synchronize operation to a clock.
20. During wafer sort good die are marked with an ink dot.
For each of the following questions, choose the best response. (6 points each)

21. A VLSI designer plans to pipeline a data path using D-type flip-flops with $t_{\text{clk-to-Q}} = 125$ psec and $t_{\text{setup}} = 125$ psec. If a 1 GHz clock is used with a maximum clock skew of 100 psec, and the worst case gate delay is 75 psec, then what is the maximum number of logic gates that can be used between flip-flops?
   
   a) 7  
   b) 8  
   c) 9  
   d) 10 
   e) 11

22. If the flip-flops in problem 21 have $t_{\text{hold}} = 150$ psec, what is the minimum number of logic gates that must be used between flip-flops?
   
   a) 0  
   b) 1  
   c) 2  
   d) 3  
   e) 4

23. If the flip-flops in problem 21 have $t_{\text{setup}} = 150$ psec and 5 logic gates are used between flip-flops, what is the timing margin for setup time analysis?
   
   a) 50 psec  
   b) 150 psec  
   c) 200 psec  
   d) 250 psec  
   e) 350 psec

24. If the clock used in problem 21 is decreased to 500 MHz with a worst case clock skew of 125 psec, and 2 logic gates are used between flip-flops, what is the timing margin for hold time analysis?
   
   a) 100 psec  
   b) 50 psec  
   c) 0 psec  
   d) -50 psec  
   e) -100 psec

25. If a 1024k x 8 SRAM uses a dual core arrangement with 64 8-bit words per word line, the number of bits required to address the word lines is:
   
   a) 10  
   b) 11  
   c) 12  
   d) 13  
   e) 14
26. A DRAM cell uses a storage capacitor of 35 fF, \( V_{DD} = 2.5\text{V} \) and \( V_T = 0.5\text{V} \) for the NMOS access FET. If \( I_{leakage} = 50 \text{ pA} \), the bit line capacitance is 315 fF, and the sense amp can detect a minimum of 50mV as a valid one, what is the maximum time between refresh cycles?
   
   a) 100 \( \mu \text{sec} \)  
   b) 500 \( \mu \text{sec} \)  
   c) 750 \( \mu \text{sec} \)  
   d) 1500 \( \mu \text{sec} \)  
   e) none of the above

27. In the ROM shown at right, what code is stored in row 4?
   
   a) 00101100  
   b) 00110100  
   c) 11011000  
   d) 01101010  
   e) none of the above

28. In the ROM shown at right, if \( k'_N = 3 k'_P \), \( V_{DD}=2.5V \), \( |V_{TP}| = V_{TN} = 0.5\text{V} \) and \( W/L_N = 2 \), then the \( W/L_P \) needed to set \( V_{OL} = 200\text{mV} \) is:
   
   a) 1.15  
   b) 1.75  
   c) 2.00  
   d) 2.25  
   e) none of the above

29. If a 91 stage ring oscillator built from inverters oscillates at 100 MHz, what is the gate delay of the inverters?
   
   a) 55 psec  
   b) 75 psec  
   c) 110 psec  
   d) 150 psec  
   e) none of the above

30. What is the output voltage for the 3-input dynamic NAND shown at right for an input of \( a = 1, b = 0, c = 0 \)? Use \( V_{DD} = 3.0\text{V} \), \( C_{out} = 125\text{fF} \), and all intermediate nodes have a capacitance of 25fF.
   
   a) 3.0 \( \text{V} \)  
   b) 2.5 \( \text{V} \)  
   c) 2.0 \( \text{V} \)  
   d) 1.5 \( \text{V} \)  
   e) none of the above

31. **BONUS** : (6 points) If a 50pA leakage current exists at the output node in the dynamic NAND in problem 30 above, the output voltage would be:
   
   a) higher  
   b) the same  
   c) lower  
   d) indeterminate  
   e) none of the above