For each of the following questions, choose the best response. (2 points each)

1. “Clock skew” is caused by:
   a) The resistance of the clock distribution lines.
   b) The capacitance of the clock distribution lines.
   c) Different lengths of the clock distribution lines.
   d) Different numbers of logic gates connected to each of the clock distribution lines.
   e) All of the above.

2. “Clock trees” are:
   a) Laid out on a chip in an “H” shape.
   b) Used to equalize the distances between the clock source and the logic gates using the clocks.
   c) Used to equalize the delays between the clock source and the logic gates using the clocks.
   d) Inserted in a place & route block before other logic gates are placed.
   e) None of the above.

3. “Pipelining” of data paths allows:
   a) More logic gates to be placed between registers.
   b) Lower power dissipation.
   c) Lower latency.
   d) Higher clock frequencies to be used.
   e) All of the above.

4. Hold time violations can be caused by:
   a) Too many logic gates placed between registers.
   b) Too few logic gates placed between registers.
   c) Large flip-flop clock-to-Q delays.
   d) Large flip-flop setup times.
   e) None of the above.

5. Which of the following advanced CMOS techniques cause static power to be dissipated?
   a) Mirror logic circuits.
   b) Pseudo-NMOS logic circuits.
   c) Tri-state logic circuits.
   d) Domino logic circuits.
   e) None of the above.

6. Which of the following are a disadvantage of dynamic logic?
   a) Charge leakage.
   b) Charge sharing.
   c) Limited clock frequency.
   d) Increased errors due to crosstalk.
   e) All of the above.
7. In an SRAM memory array:
   a) Activating a word line turns on all the bit cells in a column.
   b) Activating a word line turns on only a single word.
   c) Data is stored as charge on a capacitor.
   d) Words are often interdigitated to increase density.
   e) None of the above.

8. Compared to SRAM memories, DRAMs have the following advantages:
   a) Smaller bit cell size.
   b) Reduced errors due to leakage currents.
   c) Reduced power dissipation.
   d) Faster speed.
   e) None of the above.

9. After a silicon wafer is processed, it is tested to determine:
   a) If the processing steps were performed correctly.
   b) Which chips contain process defects.
   c) Which chips are grossly functional.
   d) Which chips meet specifications.
   e) All of the above.

10. Chips are typically “burned in” to detect failures due to:
    a) Infant mortality.
    b) Random failures.
    c) Wear-out failures.
    d) All of the above.
    e) None of the above.

For each of the following, choose either: a) True or b) False (2 points each)

11. “Sense amplifiers” are used in DRAMs because charge sharing between the bit line and storage capacitor reduce the voltage swing on the bit line, but are not needed in SRAMs.

12. Flip-flop setup and hold times are used to prevent metastability errors.

13. Pseudo-NMOS circuits are an example of “ratioed logic”.

14. The throughput of a pipelined data path can be increased by using both edges of the clock.

15. Tri-state buffers have a high impedance output state which can be used to allow multiple signals to share a single interconnect buss.

16. Domino logic uses charge-keeper circuits to avoid errors due to leakage currents.

17. “Hand shaking” is often used between major blocks on a VLSI chip to eliminate clock skew.

18. E²PROMs store data by trapping hot electrons on floating gates to shift the FET’s threshold voltage.

19. During testing a “wafer map” is often created to show the positions of all bad chips found on the wafer as an aid to debug.

20. During wafer sort a “test probe” is used to test all the chips on the wafer at once.
For each of the following questions, choose the **best** response. (6 points each)

21. A VLSI designer plans to pipeline a data path using D-type flip-flops with $t_{\text{clk-to-Q}} = 200$ psec and $t_{\text{setup}} = 250$ psec. If a 400 MHz clock is used with a maximum clock skew of 200 psec, and the typical gate delay is 150 psec, then what is the maximum number of logic gates that can be used between flip-flops?
   a) 11  
   b) 12  
   c) 13  
   d) 14  
   e) 15

22. If the flip-flops in problem 21 have $t_{\text{hold}} = 250$ psec, what is the minimum number of logic gates that must be used between flip-flops?
   a) 0  
   b) 1  
   c) 2  
   d) 3  
   e) 4

23. If the clock used in problem 21 is increased to 500 MHz, what is the maximum number of logic gates that can be used between flip-flops?
   a) 6  
   b) 7  
   c) 8  
   d) 9  
   e) 10

24. A clock is routed to two flip-flops using a single metal line. The first flip-flop is 200 µm from the clock source and the second is 600 µm from the clock source. If the delay from the clock source to the first flip-flop is 2 psec, how much clock skew will there be between the two flip-flops?
   a) 4 psec  
   b) 6 psec  
   c) 12 psec  
   d) 16 psec  
   e) 18 psec

25. If a 512k x 8 SRAM chip uses a dual core arrangement with 128 8-bit words per word line, the number of bits required to address the word lines is:
   a) 9  
   b) 10  
   c) 11  
   d) 12  
   e) 13
26. A DRAM cell uses a storage capacitor of 50 fF, $V_{DD} = 3.3\text{V}$ and $V_T = 0.8\text{V}$ for the NMOS access FET. If $I_{leakage} = 10 \text{pA}$ and the bit line capacitance is 450 fF, what voltage must the sense amp detect as a valid one after 10 msec for the memory to work properly?

a) 10 mV  
b) 50 mV  
c) 100 mV  
d) 150 mV  
e) 250 mV

27. For the DRAM cell in problem 26, if the minimum voltage the sense amp can detect as a valid one is 150 mV and the memory is refreshed at a 1 kHz rate, what is the maximum leakage current that can be tolerated?

a) 1 pA  
b) 5 pA  
c) 10 pA  
d) 50 pA  
e) 100 pA

28. When row 7 in the ROM shown at right is addressed, the output code is:

a) 0100  
b) 1010  
c) 0001  
d) 0111  
e) 1001

29. The function implemented by the logic gate shown at right is:

a) $a \cdot b$  
b) $c + d$  
c) $a \cdot b \cdot (c + d)$  
d) a) and b) above  
e) a) and c) above

30. For the logic gate shown at right, assume $V_{DD} = 3 \text{V}$, all nodes except the outputs have parasitic capacitances of 10 fF on them, and the outputs drive load capacitances of 40 fF each. When $\bar{O} = 1$ and $abcd = 1000$ the voltage on node F is:

a) 3.0 V  
b) 2.7 V  
c) 2.4 V  
d) 1.5 V  
e) 0.0 V

**BONUS** : (6 points) Methods presently in use for CMP endpoint detection include:

a) optical  
b) motor current  
c) vibration  
d) a) and b)  
e) all of the above