For the following questions, circle the best response. (20 points)

1. If a NAND gate is sized to set $\beta_n = \beta_p$, will it’s rise or fall time be faster?
   
   \begin{align*}
   \text{Rise} & \quad \text{Fall} \quad \text{Same} \quad \text{Indeterminate} \\
   \end{align*}

2. If a NOR gate is sized to set $\beta_n = \beta_p$, it’s midpoint voltage will be:
   
   \begin{align*}
   > \text{Vdd}/2 & \quad = \text{Vdd}/2 \quad < \text{Vdd}/2 \quad \text{Indeterminate} \\
   \end{align*}

3. If both a NAND gate and a NOR gate are sized to have equal trip points, which will require more silicon area?
   
   \begin{align*}
   \text{NAND} & \quad \text{NOR} \quad \text{Same} \quad \text{Indeterminate} \\
   \end{align*}

4. If the VTC for a 2 input CMOS gate shifts to the left when both inputs are switched at the same time compared to when only one is switched, that gate is a:
   
   \begin{align*}
   \text{NAND} & \quad \text{NOR} \quad \text{Either} \quad \text{Indeterminate} \\
   \end{align*}

5. If the fan-out of a NOR gate increases by 3x, it’s gate delay will increase by:
   
   \begin{align*}
   < 3x & \quad 3x \quad > 3x \quad \text{Indeterminate} \\
   \end{align*}

6. If both a 3-input NAND and a 3-input NOR drive equal load capacitances, which will use more power? Assume all FETs are the same size and have equal PN junction capacitances.
   
   \begin{align*}
   \text{NAND} & \quad \text{NOR} \quad \text{Same} \quad \text{Indeterminate} \\
   \end{align*}

7. Compared to the size of a ripple carry adder, a carry look-ahead adder is typically:
   
   \begin{align*}
   \text{Smaller} & \quad \text{Larger} \quad \text{Same} \quad \text{Indeterminate} \\
   \end{align*}

8. Which of the following circuits does not use positive feedback?
   
   \begin{align*}
   \text{R/S latch} & \quad \text{ripple carry adder} \quad \text{Ring oscillator} \quad \text{Toggle flip-flop} \\
   \end{align*}

9. If an interconnect line is moved to a lower metal layer, the delay of the line will typically get:
   
   \begin{align*}
   \text{Larger} & \quad \text{Smaller} \quad \text{Same} \quad \text{Indeterminate} \\
   \end{align*}

10. If the width of a metal interconnect line is decreased, it’s capacitance will decrease and the delay through the line will get:
    
    \begin{align*}
    \text{Larger} & \quad \text{Smaller} \quad \text{Same} \quad \text{Indeterminate} \\
    \end{align*}
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Rotate shifter __J__

12. Transparent latch __P__

13. Lumped-element model __G__

14. Ground bounce __B__

15. Sidewall capacitance __I__

A. A type of shift register which selects N out of M input bits as it's output.

B. A variation in the voltage of an on-chip power supply bus due to the inductance of the bond wires.

C. A circuit model for an interconnect line which lumps ½ the line's capacitance on either end of the line's resistance.

D. A type of latch which changes its output as soon as its input changes.

E. A variation in the voltage of an on-chip power supply bus due to the capacitance of the bus.

F. A type of latch which uses cross-coupled NAND or NOR gates.

G. A circuit model for an interconnect line which lumps the line's capacitance on the end of the line's resistance.

H. Capacitance due to the diffusion of sources and drains under poly gates.

I. Capacitance due to the perimeters of source and drain diffusions.

J. A type of shift register which wraps bits pushed out into locations emptied by the shift.
16. (20 points) (a) Find the midpoint voltage for simultaneous switching for a 3-input CMOS NOR gate with $V_{dd} = 3V$, $W_0 = W_N = 1\mu m$, $L_0 = L_N = 6.5\mu m$, $k'_{N} = 120\mu A/V^2$, $k'_{P} = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$. (b) Sketch the VTC for this case. Be sure to label all important points on your curve.

(a) $V_M = \frac{V_{dd} - V_{TP}}{1 + N \left( \frac{V_{TN}}{V_{dd}} \right)}$, \[ \text{WHERE! } \beta = \left( \frac{\pi}{2} \right)^2 \]

Here, \( \left( \frac{W}{L} \right)_N = \frac{1}{0.5} \Rightarrow \frac{\beta_N}{\beta_P} = \frac{\left( \frac{W}{L} \right)_N \beta_N}{\left( \frac{W}{L} \right)_P \beta_P} = \frac{1}{40} = \frac{3}{120} \)

\[ V_M = \frac{3 - 0.6 + 3\sqrt{3}(0.6)}{1 + 3\sqrt{3}} \]

\[ = 0.89 \text{ V} = V_M \]

(b) \[ \text{Slope of } V_{out} = -1 \text{ AT A, B} \]

\[ 0.89 \text{ V AS FOUND IN PART (a)} \]
17. (20 points) Find the worst case full time for the circuit shown below. Use \( W_B = W_N = 2 \mu m \), \( L_B = L_N = 0.5 \mu m \), \( VDD = 3 V \), \( k_N = 120 \mu A/V^2 \), \( k_P = 40 \mu A/V^2 \), \( V_{NN} = 0.6 V \), \( V_{TP} = -0.6 V \), \( C_{OX} = 6 \text{ fF/}\mu \text{m}^2 \) and all source/drain PN junction capacitances = 2 fF each. Assume \( C_i = 0 \).

\[
\text{1st, Find } C_{\text{GATE}}:
\]
\[
C_{\text{GATE}} = WLC_{\text{OX}} = (2)(0.5)(6) = 6 \text{ fF} = C_{\text{GATE}} \quad \text{ (total gate cap)}
\]

\[
\text{2nd, Find } R_{ON}:
\]
\[
R_{ON} = \frac{1}{B(V_{GS}-V_{TI})} = \frac{1}{(10)(10\times10^6)(3-0.6)} = 3.68 \text{ k}\Omega
\]

Now, worst case pull down path is as shown, through 5 series NMOS FETs with 4 intermediate nodes → use Elmore rule!

\[
\Rightarrow \tau = 5RC_{\text{OUT}} + 4RC_1 + 3RC_2 + 2RC_3 + RC_4
\]

Also, note that \( C_{\text{OUT}} = C_1 = C_2 = C_3 = 3\text{fF/}\mu \text{m}^2 + 2(C_{\text{GATE}}/2) \) (3 FETs touching each of these nodes!)

\[
\Rightarrow C_{\text{OUT}} = C_1 = C_2 = C_3 = 3(2\text{fF}) + 2(6\text{fF}) = 12\text{fF}
\]

Add, \( C_4 = 2C_{\text{GATE}}/2 = 10\text{fF} \) (1 less FET on C4 node)

\[
\Rightarrow \tau = (5R + 4R + 3R + 2R)(12\text{fF}) + R(10\text{fF})
\]

\[
\tau = (14R + 10)R = (178\text{fF})(368\Omega) = 155\text{\mu s}
\]

And, \( \tau_P = 2.2\tau = 340\text{\mu s} \)
18. (20 points) Sketch the gate-level schematic for an 8-input MUX using only CMOS inverters and NOR gates with 4 inputs or less.

Since only 4 inputs are allowed, use two 4-input MUXes followed by a 2 input MUX. Also, note that 8 inputs requires 3 bits to select which input to MUX out.

Note! Other solutions exist!

<table>
<thead>
<tr>
<th>S_2 S_1 S_0</th>
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</thead>
<tbody>
<tr>
<td>0 0 0</td>
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(Truth table for info only; not required!)
BONUS (5 points) Explain why the delay through a line decreases as its width increases. Be sure to discuss the effects of both the resistance and capacitance of the line on the delay.

The delay through an interconnect line depends on its time constant, $\tau \approx \frac{1}{2} R_{\text{line}} C_{\text{line}}$. As the width of the line increases, $R_{\text{line}}$ decreases according to $R_{\text{line}} = R_{s} \left( \frac{W}{W_0} \right)$. The capacitance increases, but not as fast as $R_{\text{line}}$ decreases, leading to a smaller $\tau$.

This is because, although the area component of the capacitance is proportional to the width of the line, the fringe component is constant.

$\Rightarrow$ As $W$ increases, $C_{\text{line}}$ increases more slowly than $R_{\text{line}} \downarrow \Rightarrow \tau \downarrow$.