For the following questions, circle the best response. (20 points)

1. If a NAND gate is sized to set $\beta_N = \beta_P$, will its rise or fall time be faster?
   
   Rise   Fall   Same   Indeterminate

2. If a NOR gate is sized to set $\beta_N = \beta_P$, it’s midpoint voltage will be:
   
   $>$ Vdd/2   = Vdd/2   $<$ Vdd/2   Indeterminate

3. If both a NAND gate and a NOR gate are sized to have equal trip points, which will require more silicon area?
   
   NAND   NOR   Same   Indeterminate

4. If the VTC for a 2 input CMOS gate shifts to the left when both inputs are switched at the same time compared to when only one is switched, that gate is a:
   
   NAND   NOR   Either   Indeterminate

5. If the fan-out of a NOR gate increases by 3x, it’s gate delay will increase by:
   
   $<$ 3x   3x   $>$ 3x   Indeterminate

6. If both a 3-input NAND and a 3-input NOR drive equal load capacitances, which will use more power? Assume all FETs are the same size and have equal PN junction capacitances.
   
   NAND   NOR   Same   Indeterminate

7. Compared to the size of a ripple carry adder, a carry look-ahead adder is typically:
   
   Smaller   Larger   Same   Indeterminate

8. Which of the following circuits does not use positive feedback?
   
   R/S latch   ripple carry adder   Ring oscillator   Toggle flip-flop

9. If an interconnect line is moved to a lower metal layer, the delay of the line will typically get:
   
   Larger   Smaller   Same   Indeterminate

10. If the width of a metal interconnect line is decreased, it’s capacitance will decrease and the delay through the line will get:
    
    Larger   Smaller   Same   Indeterminate
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Rotate shifter ________
12. Transparent latch ________
13. Lumped-element model ________
14. Ground bounce ________
15. Sidewall capacitance ________

A. A type of shift register which selects N out of M input bits as its output
B. A variation in the voltage of an on-chip power supply buss due to the inductance of the bond wires.
C. A circuit model for an interconnect line which lumps ½ the line’s capacitance on either end of the line’s resistance.
D. A type of latch which changes its output as soon as its input changes.
E. A variation in the voltage of an on-chip power supply buss due to the capacitance of the buss.
F. A type of latch which uses cross-coupled NAND or NOR gates.
G. A circuit model for an interconnect line which lumps the line’s capacitance on the end of the line’s resistance.
H. Capacitance due to the diffusion of sources and drains under poly gates.
I. Capacitance due to the perimeters of source and drain diffusions.
J. A type of shift register which wraps bits pushed out into locations emptied by the shift.
16. (20 points) (a) Find the midpoint voltage for simultaneous switching for a 3-input CMOS NOR gate with $V_{DD} = 3V$, $W_P = W_N = 1\mu m$, $L_P = L_N = 0.5\mu m$, $k'_N = 120\mu A/V^2$, $k'_P = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$, (b) Sketch the VTC for this case. Be sure to label all important points on your curve.
17. (20 points) Find the worst case fall time for the circuit shown below. Use $W_P = W_N = 2\mu m$, $L_P = L_N = 0.5\mu m$, $V_{DD} = 3V$, $k'_N = 120\mu A/V^2$, $k'_P = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$, $C_{OX} = 6 \text{ fF/}\mu \text{m}^2$ and all source/drain PN junction capacitances = 2 fF each. Assume $C_L = 0$. 

![Circuit Diagram](image)
18. (20 points) Sketch the gate-level schematic for an 8-input MUX using only CMOS inverters and NOR gates with 4 inputs or less.
BONUS (5 points) Explain why the delay through a line decreases as it’s width increases. Be sure to discuss the effects of both the resistance and capacitance of the line on the delay.