For the following questions, circle the best response. (20 points)

1. If a NOR gate is sized to set \( \beta_n = \beta_p \), will it’s rise or fall time be faster?
   - Rise: Fall, Same, Indeterminate

2. If a NAND gate is sized to set \( \beta_n = \beta_p \), its midpoint voltage will be:
   - \( > \frac{V_{dd}}{2} \) = \( \frac{V_{dd}}{2} \) < \( \frac{V_{dd}}{2} \) Indeterminate

3. If both a NAND gate and a NOR gate are sized to have equal gate delays, which will require less silicon area?
   - NAND, NOR, Same, Indeterminate

4. If the VTC for a 2-input CMOS gate shifts to the right when both inputs are switched at the same time compared to when only one is switched, that gate is a:
   - NAND, NOR, Either, Indeterminate

5. If the fan-out of a NAND gate increases by 2x, it’s gate delay will increase by:
   - \( < 2x \) 2x > 2x Indeterminate

6. If both a 2-input NAND and a 2-input NOR drive equal load capacitances, which will use more power? Assume all FETs are the same size and have equal PN junction capacitances.
   - NAND, NOR, Same, Indeterminate

7. Compared to the speed of a carry-look-ahead adder, a ripple carry adder is typically:
   - Faster, Slower, Same, Indeterminate

8. Which of the following circuits use positive feedback?
   - R/S latch, D Flip-Flop, Ring oscillator, All of these

9. If an interconnect line is moved to a higher metal layer, the delay of the line will typically get:
   - Larger, Smaller, Same, Indeterminate

10. If the width of a metal interconnect line is increased, its capacitance will increase and the delay through the line will get:
    - Larger, Smaller, Same, Indeterminate
For the following questions, choose the best definition for each word or phrase. (20 points)

11. ECO route: E
12. Barrel shifter: J
13. Fringe lines: A
14. π - model: P
15. Overlap capacitance: J

A. Electric field lines coupling from the sides of a metal interconnect line to another metal line.
B. A new place & route layout created to correct an error.
C. Capacitance due to the perimeters of source and drain diffusions.
D. A circuit model for an interconnect line which lumps ½ the line’s capacitance on either end of the line’s resistance.
E. A minor change to an existing place & route layout to correct an error.
F. Electric field lines coupling from the bottom of a metal line to the top of a metal line below it.
G. A type of shift register which wraps bits pushed out into locations emptied by the shift.
H. A circuit model for an interconnect line which lumps the line’s capacitance on the end of the line’s resistance.
I. A type of shift register which selects N out of M input bits as it’s output
J. Capacitance due to the diffusion of sources and drains under poly gates.
16. (20 points) (a) Find the midpoint voltage for simultaneous switching for a 3-input CMOS NAND gate with $V_{DD} = 3V$, $W_P = W_N = 1\mu m$, $L_P = L_N = 0.5\mu m$, $k_N = 120\mu A/V^2$, $k_P = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$. (b) Sketch the VTC for this case. Be sure to label all important points on your curve.

$$V_m = \frac{V_{PP} - N \phi I_P + \frac{1}{N} \sqrt{N \phi I_P} V_{TN}}{\frac{1}{N} \sqrt{N \phi I_P}}$$

WHERE: $\phi = \left( \frac{V}{L} \right) \frac{L_N}{L_P}$

WHERE: $\frac{V}{L} = \left( \frac{W}{L} \right) N = 1/0.5 \Rightarrow \phi = \left( \frac{W}{L} \right) N = \frac{L_N}{L_P} = \frac{120}{40} = 3$

$$V_m = 3 - 0.6 + \frac{1}{3} \sqrt{3} (0.6) = 1.74V = V_m$$

(b)

Diagram:

- $V_{OUT}$ vs $V_{IN}$
- $V_{OH} = \left( \frac{1}{3} \right) V_{PP}$
- $V_{OH} = 1.74V$
- $V_{OL} = 0$
- $V_{IL} = 1.74V$
- $V_{IN}$
- $V_{PP} = 3V$
- Slope of $V_{OUT} = -1$ at $A, B$

As found in Part (a)
17. (20 points) Find the worst case rise time for the circuit shown below. Use \( W_p = W_n = 2 \mu m \), \( L_p = L_n = 6.5 \mu m \), \( V_{DD} = 3V \), \( k_n = 120 \mu A/V^2 \), \( k_p = 40 \mu A/V^2 \), \( V_{TN} = 0.6V \), \( V_{TP} = -0.6V \), \( C_{OX} = 6 \text{ fF}/\mu m^2 \) and all source/drain PN junction capacitances \( 2 \text{ fF} \) each. Assume \( C_t = 0 \).

**WORST CASE PATH FOR \( \tau_R \)**

1st, find \( C_{GATE} \):

\[ C_{GATE} = W \cdot L \cdot C_{OX} = (2)(0.5) \text{ fF} = 2 \text{ fF} \]

\[ C_{GATE} = 2 \text{ fF} = \text{TOTAL GATE CAP FOR ALL FETS} \]

Now, worst case pull up path is as shown, through \( 4 \) series PMOS FETs with 3 intermediate nodes. USE ELMORE RULE!

\[ \gamma = (R_1 + R_2 + R_3 + R_4) \cdot C_{OUT} \]

\[ + (R_1 + R_3 + R_4) \cdot C_3 \]

\[ + (R_1 + R_4) \cdot C_2 \]

\[ + R_1 \cdot C_1 \]

Now, note that \( C_1 = C_2 = C_3 = 3C_{OX} + 2 \cdot \frac{C_{GATE}}{2} = 3(2 \text{ fF}) + 2 \cdot \frac{2 \text{ fF}}{2} = 12 \text{ FF} \)

\[ C_1 = C_2 = C_3 = 12 \text{ FF} \]

Also, \( C_{OUT} = \text{SAME!} \) (3 PMOS in series)

\[ \gamma = \frac{1}{12 \text{ FF}} \cdot \left( \frac{1}{(1/2) \cdot (0.5 \times 10^{-6}) (3-0.6)} \right) = 2.6 \text{ k\Omega} \]

\[ R_1 = R_2 = R_3 = R_4 = \frac{1}{(0.6)(0.5 \times 10^{-6}) (3-0.6)} = 2.6 \text{ k\Omega} \]

\[ \Rightarrow \gamma = 4R_1 \gamma + 8R_1 \gamma + 2R_1 \gamma + R_1 \gamma \]

\[ \gamma = 10R_1 \gamma \]

\[ \gamma = 10R_1 \gamma \]

\[ \gamma = 2.2 \gamma = 6.86 \text{ psec} \]

AND, \( \frac{1}{\tau_R} = 2.2 \gamma = 6.86 \text{ psec} \)
18. (20 points) Sketch the gate-level schematic for an 8-input MUX using only CMOS inverters and NAND gates with 4 inputs or less.

**Since only 4 inputs are allowed, use 2 4-input MUXes followed by a 2-input MUX. Also, note that 8 inputs requires 3 bits to select which of the inputs to MUX out.**

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CROSSTALK OCCURS WHEN ONE SIGNAL CAPACITIVELY COUPLES TO ANOTHER SIGNAL, FOR EXAMPLE BETWEEN TWO CLOSELY SPACED METAL INTERCONNECT LINES.

IF THE TWO SIGNALS ARE SWITCHING IN OPPOSITE DIRECTIONS (LOW-TO-HIGH VS. HIGH-TO-LOW), THEN THIS CAPACITANCE MUST BE CHARGED AS WELL, SLOWING DOWN RISE & FALL TIMES. IF THE 2 SIGNALS ARE SWITCHING IN THE SAME DIRECTION, THEN THIS CAP DOESN'T NEED TO BE CHARGED (SAME VOLTAGE ON BOTH SIDES), WHICH SPEEPS UP RISE & FALL TIMES.