For the following questions, circle the best response. (20 points)

1. If a NOR gate is sized to set $\beta_N = \beta_P$, will it’s rise or fall time be faster?
   
   Rise    Fall    Same    Indeterminate

2. If a NAND gate is sized to set $\beta_N = \beta_P$, it’s midpoint voltage will be:
   
   > Vdd/2    = Vdd/2    < Vdd/2    Indeterminate

3. If both a NAND gate and a NOR gate are sized to have equal gate delays, which will require less silicon area?
   
   NAND    NOR    Same    Indeterminate

4. If the VTC for a 2 input CMOS gate shifts to the right when both inputs are switched at the same time compared to when only one is switched, that gate is a:
   
   NAND    NOR    Either    Indeterminate

5. If the fan-out of a NAND gate increases by 2x, it’s gate delay will increase by:
   
   < 2x    2x    > 2x    Indeterminate

6. If both a 2-input NAND and a 2-input NOR drive equal load capacitances, which will use more power? Assume all FETs are the same size and have equal PN junction capacitances.
   
   NAND    NOR    Same    Indeterminate

7. Compared to the speed of a carry look-ahead adder, a ripple carry adder is typically:
   
   Faster    Slower    Same    Indeterminate

8. Which of the following circuits use positive feedback?
   
   R/S latch    D Flip-Flop    Ring oscillator    All of these

9. If an interconnect line is moved to a higher metal layer, the delay of the line will typically get:
   
   Larger    Smaller    Same    Indeterminate

10. If the width of a metal interconnect line is increased, it’s capacitance will increase and the delay through the line will get:
    
    Larger    Smaller    Same    Indeterminate
For the following questions, choose the best definition for each word or phrase. (20 points)

11. ECO route ________
12. Barrel shifter ________
13. Fringe lines ________
14. \(\pi\) - model ________
15. Overlap capacitance ________

A. Electric field lines coupling from the sides of a metal interconnect line to another metal line.

B. A new place & route layout created to correct an error.

C. Capacitance due to the perimeters of source and drain diffusions.

D. A circuit model for an interconnect line which lumps \(\frac{1}{2}\) the line’s capacitance on either end of the line’s resistance.

E. A minor change to an existing place & route layout to correct an error.

F. Electric field lines coupling from the bottom of a metal line to the top of a metal line below it.

G. A type of shift register which wraps bits pushed out into locations emptied by the shift.

H. A circuit model for an interconnect line which lumps the line’s capacitance on the end of the line’s resistance.

I. A type of shift register which selects \(N\) out of \(M\) input bits as it’s output

J. Capacitance due to the diffusion of sources and drains under poly gates.
16. (20 points) (a) Find the midpoint voltage for simultaneous switching for a 3-input CMOS NAND gate with $V_{DD} = 3V$, $W_P = W_N = 1\mu m$, $L_P = L_N = 0.5\mu m$, $k'_N = 120\mu A/V^2$, $k'_P = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$, (b) Sketch the VTC for this case. Be sure to label all important points on your curve.
17. (20 points) Find the worst case rise time for the circuit shown below. Use $W_P = W_N = 2\mu m$, $L_P = L_N = 0.5\mu m$, $V_{DD} = 3V$, $k'N = 120\mu A/V^2$, $k'P = 40\mu A/V^2$, $V_{TN} = 0.6V$, $V_{TP} = -0.6V$, $C_{OX} = 6 \text{ fF/}\mu \text{m}^2$ and all source/drain PN junction capacitances = 2 fF each. Assume $C_L = 0$. 

![Circuit Diagram]
18. (20 points) Sketch the gate-level schematic for an 8-input MUX using only CMOS inverters and NAND gates with 4 inputs or less.
BONUS (5 points) Explain how crosstalk can affect rise and fall times.