For the following questions, circle the best response. (20 points)

1. PMOS FETs used as switches can only pass a “weak”:
   - logic 1
   - logic 0
   - both 1 & 0
   - neither 1 or 0

2. Compared to the number of NMOS FETs in a CMOS logic gate, the number of PMOS FETs is:
   - Greater
   - Smaller
   - Same
   - Indeterminate

3. To implement an “and” function in a complex CMOS gate, the NMOS FETs are placed in:
   - Parallel
   - Series
   - Both
   - Indeterminate

4. “Moore’s Law” predicts that the number of transistors on a chip will double every:
   - 1 year
   - 2 years
   - 4 years
   - 6 years

5. Compared to the mobility of electrons in silicon, the mobility of holes is:
   - Larger
   - Smaller
   - The same
   - Indeterminate

6. A “Class 10” clean room will have < 10 particles in the air per cubic:
   - cm
   - meter
   - inch
   - foot

7. As a CMOS process gets more mature, the yield of a chip:
   - Increases
   - Decreases
   - No Change
   - Indeterminate

8. Which of the following materials is NOT always deposited in a CMOS process:
   - Silicon nitride
   - Polysilicon
   - Silicon dioxide
   - Aluminum

9. As Vgs increases across an FET, “channel length modulation” causes drain current to:
   - Increase
   - Decrease
   - No Change
   - Indeterminate

10. Gate leakage is caused by which of the following:
    - Hot carriers
    - Punch-through
    - Tunneling
    - Sub-threshold slope
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Reticle ___
12. Impact ionization ___
13. Overglass ___
14. DIBL ___
15. Straggle ___

A. A short channel effect in MOSFETs which causes mobility to decrease as $V_{GS}$ increases.
B. The standard deviation of a gaussian ion implant profile.
C. The geometric pattern used to align one mask layer to the next.
D. The step in a CMOS process used to deposit insulator between metal layers.
E. The mean of a gaussian ion implant profile.
F. A short channel effect in MOSFETs which causes $V_T$ to decrease as $V_{DS}$ increases.
G. A hot carrier effect in MOSFETs which causes $V_T$ to shift over time.
H. The multi-chip pattern which is stepped across a wafer.
I. The step in a CMOS process used to protect the finished chip from moisture and contaminants.
J. A hot carrier effect in MOSFETs which causes substrate current at high values of $V_{DS}$. 
16. (20 points) (a) On the layout diagram below indicate the metal connections required to implement the function \( F = \overline{A \oplus B} \). Assume that both inverted and non-inverted inputs are available and label each poly gate with the input used.

![Layout Diagram](image)

(b) Draw the schematic for the logic gate above.

\[ F = \overline{A \oplus B} = \text{"EXCLUSIVE NOR"} = \overline{A} \cdot \overline{B} + \overline{A} \overline{B} \]

\[ \text{\textit{SAD} GATE USED FOR XNOR} \]

\[ \text{\textit{NOTE: OTHER SOLUTIONS EXIST}} \]
17. (20 points) For the inverter shown below with its output shorted to its input, find the value of \( W/L_N \) needed to set \( V_{out} = 1 \) V if \( W/L_P = 1 \). Use: \( V_{DD} = 3 \) V, \( k_N = 120 \mu A/V^2 \), \( k_P = 40 \mu A/V^2 \), \( V_{IN} = 0.5 \) V, \( V_T = -0.5 \) V. (Hint: Note that \( I_{DP} = I_{DN} \))

\[
\text{SINCE } V_{DS} = V_{GS} \text{ FOR BOTH FETS,} \]
\[
\Rightarrow \text{ BOTH NMOS & PMOS} \]
\[
\text{ARE IN SATURATION!} \]

\[
\frac{\beta_N}{2} \left( V_{DD} - V_{OUT} - V_T \right)^2 = \frac{\beta_P}{2} \left( V_{OUT} - V_{IN} \right)^2 \]

\( \text{OR, SUBSTITUTING IN VALUES} \Rightarrow \)
\[
\frac{1}{2} \left( 4 \times 10^{-6} \right) \left( 3 - 1 - 0.5 \right)^2 = \frac{1}{2} \left( \frac{V}{L} \right)_N \left( 120 \times 10^{-6} \right) \left( 1 - 0.5 \right)^2 \]
\[
\Rightarrow \left( \frac{V}{L} \right)_N = \left( 4 \times 10^{-6} \right) \left( 1.5 \right) \left( 0.5 \right) = \left( \frac{1}{2} \right) \left( 3 \right)^2 = 3 \]
\[
\Rightarrow \left( \frac{V}{L} \right)_N = 3 \]
According to the scaling theory discussed in class, predict the new values of each of the parameters below in a 90nm process based on the following values for a 0.18μm process:

- $V_{DD} = 1.8V$
- $k'_N = 240μA/V^2$
- $V_{TN} = 0.45V$
- Area of a minimum 2-input NAND gate = 10μm$^2$
- Delay of a minimum 2-input NAND gate = 100 ps

### 0.18μm Values

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>1.8V</td>
</tr>
<tr>
<td>$k'_N$</td>
<td>240μA/V^2</td>
</tr>
<tr>
<td>$V_{TN}$</td>
<td>0.45V</td>
</tr>
<tr>
<td>NAND Area</td>
<td>10μm$^2$</td>
</tr>
<tr>
<td>NAND Delay</td>
<td>100 ps</td>
</tr>
</tbody>
</table>

### Scaling Rule

- $V_{DD}' = \frac{V_{DD}}{S}$
- $k'_N' = \frac{k'_N}{S}$
- $V_{TN}' = \frac{V_{TN}}{S}$
- Area' = $\frac{\text{Area}}{S^2}$
- Delay' = $\frac{\text{Delay}}{S}$

### Predicted Values for 90nm

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>0.9V</td>
</tr>
<tr>
<td>$k'_N$</td>
<td>$\frac{480μA}{V^2}$</td>
</tr>
<tr>
<td>$V_{TN}$</td>
<td>0.225V</td>
</tr>
<tr>
<td>Area</td>
<td>$2.5\mu m^2$</td>
</tr>
<tr>
<td>Delay</td>
<td>50 ps</td>
</tr>
</tbody>
</table>

Note: $\frac{0.18\mu m}{0.09\mu m} = 2 = S$
BONUS (5 points)  Explain why MOS threshold voltages typically do not scale as much as is predicted by ideal scaling theory.

\( V_T \) does not scale as much as scaling theory predicts for 2 main reasons:

1) The need to reduce leakage currents when the FETs are off, due to subthreshold current

2) The need to keep \( V_{TH} > 0 \) and \( V_{TH} < 0 \) over all process corners & temperatures