For the following questions, circle the best response. (20 points)

1. The input to a VLSI block is 01110011. If the output is 10111001, then the block’s function is:
   - Rotate Left
   - Rotate Right
   - Shift Left
   - Shift Right
   - Barrel Shift

2. The input to a VLSI block is 10110001. If the output is 01100010, then the block’s function is:
   - Rotate Left
   - Rotate Right
   - Shift Left
   - Shift Right
   - Barrel Shift

3. If both a NAND gate and a NOR gate are made with ALL minimum size MOSFETs, which will have the faster rise time?
   - NAND
   - NOR
   - Same
   - Indeterminate

4. If both a NAND gate and a NOR gate are sized to have equal rise and fall times, which will require more silicon area?
   - NAND
   - NOR
   - Same
   - Indeterminate

5. If both a NAND gate and a NOR gate are made with ALL minimum size MOSFETs, which will have the larger mid-point voltage for simultaneous switching?
   - NAND
   - NOR
   - Same
   - Indeterminate

6. Compared to a ripple carry adder, the speed of a carry look ahead adder is:
   - Faster
   - Slower
   - Same
   - Indeterminate

7. Compared to a ripple carry adder, the area of a carry look ahead adder is:
   - Larger
   - Smaller
   - Same
   - Indeterminate

8. Compared to the mobility of electrons, the mobility of holes is:
   - Larger
   - Smaller
   - Same
   - Indeterminate

9. The power used by CMOS circuits scale proportional to the square of:
   - Clock frequency
   - Supply voltage
   - Load capacitance
   - Temperature

10. If the spacing between NMOS and PMOS FETs in a output pad is decreased, the probability of latch-up will:
    - Increase
    - Decrease
    - No Change
    - Indeterminate
For the following questions, choose the **best** definition for each word or phrase. (20 points)

11. Snap-back device
   - A. The difference between \( V_{OH} \) and \( V_{OL} \) for a CMOS logic gate.
   - B. The current which flows from Vdd to the load capacitance as a CMOS logic gate switches.
   - C. A method used to calculate the delay through a CMOS logic gate.
   - D. The number of 2-input NAND gates a CMOS logic gate can drive.
   - E. A special type of device used for ESD protection on Input/Output pads.
   - F. A method used to insure the inputs to all flip-flops are stable before they are clocked.
   - G. The number of identical logic gates a CMOS logic gate can drive.
   - H. A special type of device used in high speed VLSI circuits.
   - I. The difference between \( V_{OH} \) and \( V_{IH} \) for a CMOS logic gate.
   - J. The current which flows from Vdd to ground as a CMOS logic gate switches.

12. Noise Margin
   - A. The difference between \( V_{OH} \) and \( V_{OL} \) for a CMOS logic gate.
   - B. The current which flows from Vdd to the load capacitance as a CMOS logic gate switches.
   - C. A method used to calculate the delay through a CMOS logic gate.
   - D. The number of 2-input NAND gates a CMOS logic gate can drive.
   - E. A special type of device used for ESD protection on Input/Output pads.
   - F. A method used to insure the inputs to all flip-flops are stable before they are clocked.
   - G. The number of identical logic gates a CMOS logic gate can drive.
   - H. A special type of device used in high speed VLSI circuits.
   - I. The difference between \( V_{OH} \) and \( V_{IH} \) for a CMOS logic gate.
   - J. The current which flows from Vdd to ground as a CMOS logic gate switches.

13. Fan-out
   - A. The difference between \( V_{OH} \) and \( V_{OL} \) for a CMOS logic gate.
   - B. The current which flows from Vdd to the load capacitance as a CMOS logic gate switches.
   - C. A method used to calculate the delay through a CMOS logic gate.
   - D. The number of 2-input NAND gates a CMOS logic gate can drive.
   - E. A special type of device used for ESD protection on Input/Output pads.
   - F. A method used to insure the inputs to all flip-flops are stable before they are clocked.
   - G. The number of identical logic gates a CMOS logic gate can drive.
   - H. A special type of device used in high speed VLSI circuits.
   - I. The difference between \( V_{OH} \) and \( V_{IH} \) for a CMOS logic gate.
   - J. The current which flows from Vdd to ground as a CMOS logic gate switches.

14. Shoot-through current
   - A. The difference between \( V_{OH} \) and \( V_{OL} \) for a CMOS logic gate.
   - B. The current which flows from Vdd to the load capacitance as a CMOS logic gate switches.
   - C. A method used to calculate the delay through a CMOS logic gate.
   - D. The number of 2-input NAND gates a CMOS logic gate can drive.
   - E. A special type of device used for ESD protection on Input/Output pads.
   - F. A method used to insure the inputs to all flip-flops are stable before they are clocked.
   - G. The number of identical logic gates a CMOS logic gate can drive.
   - H. A special type of device used in high speed VLSI circuits.
   - I. The difference between \( V_{OH} \) and \( V_{IH} \) for a CMOS logic gate.
   - J. The current which flows from Vdd to ground as a CMOS logic gate switches.

15. Timing analysis
   - A. The difference between \( V_{OH} \) and \( V_{OL} \) for a CMOS logic gate.
   - B. The current which flows from Vdd to the load capacitance as a CMOS logic gate switches.
   - C. A method used to calculate the delay through a CMOS logic gate.
   - D. The number of 2-input NAND gates a CMOS logic gate can drive.
   - E. A special type of device used for ESD protection on Input/Output pads.
   - F. A method used to insure the inputs to all flip-flops are stable before they are clocked.
   - G. The number of identical logic gates a CMOS logic gate can drive.
   - H. A special type of device used in high speed VLSI circuits.
   - I. The difference between \( V_{OH} \) and \( V_{IH} \) for a CMOS logic gate.
   - J. The current which flows from Vdd to ground as a CMOS logic gate switches.
16. (20 points) For the 2-input NAND gate below, calculate the worst case rise time, fall time, and propagation delay. Also calculate the mid-point voltage for simultaneous switching. Use \( W_P = 4 \mu m, W_N = 2 \mu m, L_P = L_N = 1 \mu m, \) all diffusion lengths = 2\( \mu m, \) \( L_{\text{overlap}} = 0.1 \mu m, \) \( V_{DD} = 3V, \) \( C_{OX} = 5 \text{ fF/\mu m}^2, \) \( k'_N = 120 \mu A/V^2, \) \( k'_P = 40 \mu A/V^2, \) \( V_{TN} = 0.6V, \) \( V_{TP} = -0.6V, \) \( C_{jn} = C_{jp} = 1 \text{ fF/\mu m}^2, \) \( C_{jswn} = C_{jswp} = 0.25 \text{ fF/\mu m}^2, \) \( C_{load} = 30 \text{ fF} \)
(extra work space for problem 16)
17. (20 points) Draw the schematic for a complex CMOS logic gate implementing the function 
\[ F = AB + C + D \] 
Indicate the relative W/L ratios required for all MOSFETs to equalize the 
worst case rise and fall times. Assume \( \mu_N = 3 \mu_P \)
18. (20 points) Draw the cross section of a CMOS inverter and indicate on your sketch all parasitic devices involved if this structure should latch up. Draw the schematic used to model this effect.
BONUS (5 points) List the major steps in a top-down VLSI design flow in the order they occur.