For the following questions, circle the best response. (20 points)

1. What happens to the resistance of doped silicon as the doping concentration increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

2. What happens to the width of a PN junction depletion region as the reverse bias increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

3. What happens to the magnitude of the MOS threshold voltage as the substrate doping increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

4. What happens to the gate capacitance of a MOSFET as the gate oxide thickness increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

5. What happens to the Vt of an NMOS FET as the source to body voltage increases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

6. What happens to the channel resistance of a triode MOSFET as W/L decreases?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

7. What happens to the current in a saturated NMOS FET as Vds increases beyond Vgs − Vt?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

8. According to scaling theory, what happens to the power of MOS circuits as they are scaled down?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

9. According to scaling theory, what happens to the resistance of a triode FET as it is scaled down?
   - Increases
   - Decreases
   - No Change
   - Indeterminate

10. According to scaling theory, what happens to the speed of MOSFETs as they are scaled down?
    - Increases
    - Decreases
    - No Change
    - Indeterminate
For the following questions, choose the best definition for each word or phrase. (20 points)

11. Sub-threshold slope __D__
12. Channel length modulation __J__
13. Self-aligned gate __G__
14. Photolithography __B__
15. Chemical Mechanical Polishing __I__

A. The relationship between drain current and gate voltage for a MOSFET with Vds < Vgs - Vt.
B. The process by which a pattern is transferred from a mask to the silicon surface.
C. The effect which causes some drain current to flow into the substrate at high values of Vds.
D. The relationship between drain current and gate voltage for a MOSFET with Vgs < Vt.
E. The process through which each mask is aligned to the features created by the prior mask.
F. The process used to passivate a finished chip.
G. The process by which the boundaries of the source and drain are defined by the gate.
H. The process used to repair damage to the silicon crystal caused by ion implantation.
I. The process used to planarize each interconnect layer before the next one is added.
J. The effect which causes drain current to increase as Vds is increased > Vgs - Vt.
16. (20 points) Sketch the cross-section of an NMOS FET in saturation. Label all features and show the appropriate shapes and sizes for the channel and all depletion regions.

![Diagram of NMOS FET cross-section]

Vgs > Vt
Vds > Vgs - Vt

**NOTE:** Please do not take off points if the depletion regions surrounding S & D are drawn equal (unfortunately, the book shows that!)
17. (20 points): Calculate the threshold voltage for an NMOS FET at 27°C with $t_{ox} = 50\,\text{Å}$, $N_A = 10^{16}/\text{cm}^3$, $V_{PD} = -0.5\text{V}$ and $D_t = 10^{-7}/\text{cm}^3$.

Use: $V_T = \frac{1}{C_{ox}} \left( \frac{2q_e N_A (2|\phi_f|)}{kT} + 2|\phi_f| + V_{PD} + \frac{qD_t}{C_{ox}} \right)$

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.95 \times 10^{-12}}{5 \times 10^{-8}} = 8.1 \times 10^{-9} \text{F/cm}^2 = C_{ox}$

$|\phi_f| = \frac{kT}{q} \ln \left( \frac{N_A}{n_i} \right) = \frac{(1.38 \times 10^{-23}) (273 + 27)}{1.6 \times 10^{-19}} \ln \left( \frac{10^{16}}{10^{10}} \right) = 357.5 \text{mV}$

$\Rightarrow 2|\phi_f| = 715 \text{mV}$

$\frac{1}{C_{ox}} \left[ 2q_e N_A (2|\phi_f|) \right]^2 = \left[ \frac{6.2 \times 10^{-7}}{6.9 \times 10^{-9}} \right] = 70.7 \text{mV}$

$\frac{qD_t}{C_{ox}} = \left( \frac{1.6 \times 10^{-19}}{6.9 \times 10^{-9}} \right) = 231.9 \text{mV}$

$V_T = 70.7 \text{mV} + 715 \text{mV} - 500 \text{mV} + 231.9 \text{mV} = 517.6 \text{mV}$

$V_T = 517.6 \text{mV}$
18. (20 points) On the layout diagrams below, indicate the metal connections required to create:

(a) a 2 input CMOS NAND gate

(b) a complex CMOS logic gate implementing the function \( F = AB + C + D \)

Other possible connections exist for both (a) and (b). (Schematic on bonus question next page)

Note: Schematics not required for this problem. (For reference only.)
BONUS (5 points). Draw the schematic for the complex CMOS logic gate in problem 18(b).

\[ V_{out} = AB + C + D \]