Test logic requirements.

- We need to check the 8 bit ADC output.
- We also, need to bring the 14 raw comparator bits to the output pins. (on a single clock).
- We need a way to manipulate the currents on various components of the ADC pipe stage.
- Also, bring in the current and voltage references externally.
  - We can achieve the first three objectives by sharing the output pins between the raw comparator bits and the 8 bit ADC output and by using some of the raw comparator bit pins as bidirectional pins.
  - But the last objective will require its own set of pins.
TEST LOGIC

• To make the logic idiot proof, we need a way by which only the ADC output is on the output pins or only the raw comparator bits or only the chicken dac bits are on the bidirectional pins.

• This will prevent any contention on the output pins.
I/P OR O/P mode?

en_12

RAW COMP Bits or DATA

1 0

EN

RAW COMP BITS

1 0

DATA

C_DAC

Load

1 0

Load the new C_DAC Bits

Wait for Load=1
SELECT BIT REGISTERS
BIT SELECT LATCH
ADDRESS LOGIC
25-Jul-2004  File : iref_eldonet.cou
22:27:33  ELDO v6.3_1_1 (Production version) : * Component: $ADC2/USER/kshitij/iref

- CHK DAC BITS CHANGE OVER POINTS

- CHK DAC BITS CHANGE OVER POINTS
## TEST LOGIC

<table>
<thead>
<tr>
<th>Component</th>
<th># of test bits required</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amplifier</td>
<td>3</td>
</tr>
<tr>
<td>Comparator</td>
<td>3 (used twice)</td>
</tr>
<tr>
<td>Reference Generator</td>
<td>3</td>
</tr>
<tr>
<td>Clock Generator</td>
<td>2</td>
</tr>
</tbody>
</table>
TEST LOGIC.

• Number of test bits required is 3.
• In all we need to address five sets of control units.
  – So we required 3 addressing line in all.
  – This makes the total number of pins required for the Chicken DAC control is 6.
• These pins can be shared with the raw comparator bits output pins.