ADC Design Team 2

Reference Generator Circuits

Anas Ahmad
Voltage Reference Circuit 1

Figure 1: Circuit for generating differential references voltages

Circuit Description:

- $I_{ref}$ is supplied by the band-gap reference (BGR), mirrored through M2 to a floating R1, matched with the resistors in the BGR.
- That results in the differential reference voltage across R1.
- The common mode level of $V_{ref}$ is set by op-amp feedback circuit controlling M1.
- The bias voltage $V1$ is generated with a dummy circuit.
- $V_{c}$ is adjusted so that node n3 tracks node n2.
- $V_{ref+}$ and $V_{ref-}$ are buffered with the unity gain buffers A1 and A2.
Voltage Reference Circuit 2

Circuit Description:

- Unit Resister based current
- $Vin (1.2V)$ is supplied by an off-chip BandGap circuit, and buffered by opamp1
- The op-amp forces voltage across $R1$ to equal $Vin$.
- $Id$ through $M1 = Vin / R1$.
- $Id(M1)$ is mirrored with $M2$ to go through $R2$, $R3$, and $R4$
Figure 2: Voltage Reference Generator Circuit
- Voltage across the resistors = $I_d(M1) \times R_T$
  $= (Vin / R1) \times R_T$

- Resulting Voltage is set by ratio of resistors:
  $V2= Vin \times (R_T / R1)$

- $V2$ is buffered with op-amp2 to give us the desired reference voltage $V_{ref1}$.

- Bypass caps at output to suppress supply ripples.

- Op-amp 1 is a Current Mirror op-amp that sets the common mode for M1
- **Id (M1):**
  - Keep as small as possible in order to reduce the size of M1 to keep parasitic caps small

- **External Current Switch:**
  - to supply Id for M1 leg when it’s closed from an off chip current source, incase opamp1 failed to operate
Bias Current Reference Circuit

Circuit Description:

- Generates the bias current required by other circuits on the chip.
- Behaves similar to the voltage reference circuit at the input stage.
- Reference Current is generated by setting a voltage by the opamp across a fixed external Resistor.
- This is to assure that current doesn’t vary if to use a built-in resistor, which varies due to process and temperature.
Circuit Specifications:
- Generated Reference Current = 50uA
- Current is mirrored with a cascode current mirror with ratios (1:1)
- To get 50uA from a Vin=1.2V, we need a fixed R = 24kΩ

Test Functionality of Circuit:
- Have a mirrored leg going out to a pin on the chip to measure the current.
- Make sure to include few extra current legs available incase.
Figure 3: Bias Current Reference Circuit
Op-amp Design: “Current Mirror Amplifier”

Circuit Description:

- Current is scaled from input stage to the output stage by a factor of $K$ (2~5)
- Not a very high/fast op-amp if a simple current mirrors are used
- Solution! Use Wide Swing Cascode Current mirrors to increase gain, by increasing output resistance, and swing.
- The $K$ factor cannot be increased indefinitely in order to keep the poles separated and to avoid increasing the capacitance of N.D.P
Error Budget:

- Resistors Mismatch and variations
- Current Mirror Mismatch
- Op-amp Gain Accuracy
- Supply Rejection
Simulation of V.R. Circuit

Figure 5: Test Bench for Voltage Reference Circuit
Figure 6: Simulation Results for VRC