Comparator Architecture

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Outline

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  – Advantages/Disadvantages
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  – Advantages/Disadvantages
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ADC STAGE FOR 1.5b

Raw Comparator Output

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>B1</th>
<th>B2</th>
<th>CLK2</th>
<th>MSB</th>
<th>LSB</th>
<th>VDAC+</th>
<th>VDAC-</th>
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<td>0</td>
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<td>Vref-</td>
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</table>

Vin+ —— A1 —— Device —— A2 —— Device —— CLK2 —— Device —— VDAC+ —— VDAC-
Output Waveforms of a Non-Overlapping Clock Generator.
RESISTIVE DIVIDER COMPARATOR
Comparator

**Phase 1**
Clk is high, the cross couple transistor pair is engaged from analog to digital

**Phase 2**
Clk is low and Vout+ and Vout- are both set to Vdd
If G1 > G2, the current in the left branch is more than the current in the right branch. Hence the left output capacitance will be discharged faster than the right output capacitance, i.e. Vout- decreases faster than Vout+.
Preamp Latch Comparator
Comparator

Regeneration

Step 1:
Phi2 getting low and Phi1 getting high.

Step 2:
Phi1 gets high and M8 and M9 are closed.

ADVANTAGES
TOLERABLE OFFSET
HIGH SPEED & RESOLUTION
Conclusion

The Preamplifier Latch comparator seems to be less risky for our application since the offset is much lower for this design. Although, our offset is very relaxed it is always good to have some margin.