Comparator Design

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Outline

• Introduction
  - Architecture
  - Specifications
• Schematics
• Equations
• Simulations
• Conclusion
ADC STAGE FOR 1.5b

![ADC Stage Diagram]

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>B1</th>
<th>B2</th>
<th>CLK2</th>
<th>MSB</th>
<th>LSB</th>
<th>VDAC+</th>
<th>VDAC-</th>
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<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Vref-</td>
<td>Vref+</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
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<td>VDAC-</td>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>Vref+</td>
<td>Vref-</td>
</tr>
</tbody>
</table>

[Diagram showing the ADC stage with input and output connections, comparator outputs, and a truth table for the raw comparator output.]
Output Waveforms of a Non-Overlapping Clock Generator.
Architecture & Specs

SPECIFICATIONS

Offset < 100mV
Decision time < 5ns
Power Consumption < Glowing
Test bench for final comparator
Comparator

Regeneration

Step 1: Phi2 getting low and Phi1 getting high.

Step 2: Phi1 gets high and M8 and M9 are closed.
Swing-minimizing circuit
New swing to switch M12
NAND gate
RS-Latch
Lockout Output
Lockout Output
Regeneration process equations

As the conductance of switch M12 becomes smaller than half of the transconductance of M4 and M5, the n-channel flip-flop starts the first step of regeneration.

\[ \text{gm1=transconductance from input pairs.} \]
\[ \text{gm4=transconductance from M4 or M5} \]
\[ \text{go12=conductance of M12} \]
\[
\frac{1}{2} \cdot \text{Vin} \cdot \text{gml} = \text{Ca} \cdot \frac{dV_a}{dV_b} + \text{gm4} \cdot V_b + \text{go12}(V_a - V_b)
\]

\[
-\frac{1}{2} \cdot \text{Vin} \cdot \text{gml} = \text{Ca} \cdot \frac{dV_b}{dV_b} + \text{gm4} \cdot V_b - \text{go12}(V_a - V_b)
\]

\[
V_a - V_b = [Vao - Vbo - \left(\frac{\text{gml}}{(2 \cdot \text{go12} - \text{gm4})}\right) \cdot \text{Vin}] \exp\left(\frac{t}{\tau}\right) + \left(\frac{\text{gml}}{(2 \cdot \text{go12} - \text{gm4})}\right) \cdot \text{Vin}
\]

\[
\tau = \frac{\text{Ca}}{\text{gm4} - 2 \cdot \text{go12}}
\]
Offset Equation

\[ V_{off} = V_{off1} + \left( \frac{g_m 4}{g_m 1 \times (V_{off2} + V_e)} \right) \]

Ve=Charge injection error.

Voff2=n-channel FF

Voff1=input transistor pairs

Inequality to ensure that there is still some extra current to charge both nodes at the beginning of reset time interval: \( I_{12} > I_5 \)

\[ \frac{W_{12}}{L} \times K_{pn} \left[ (V_{dd} - V_b - V_{tn12}) \times (V_a - V_b) - \frac{1}{2} \times (V_a - V_b)^2 \right] > \]

\[ \frac{W_{5}}{L} \times K_{pn} \left[ (V_a - V_{ss} - V_{tn5}) \times (V_b - V_{ss}) - 0.5 \times (V_b - V_{ss})^2 \right] \]

\[ W_{12} > \frac{1}{4} \times W_4 \]
Second period of the reset mode

\[ V_a - V_b = \left( \frac{gm1 \cdot Vin}{(2 \cdot go12 - gm4)} \right) + A \cdot \exp \left( \frac{t}{\tau} \right) \]

\[ V_a + V_b = B \cdot \exp \left( \frac{-gm4}{Ca \cdot t} \right) \]

\[ \tau = \frac{Ca}{gm4 - 2 \cdot go12} \]

Optimization Results

\[ \tau = \frac{(\alpha \cdot W4 + Cp)}{2 \cdot I4 \cdot W4} \cdot \sqrt{\frac{L4 \cdot Kpn}{\frac{1}{3} \cdot W4}} \]

\[ W12 = \frac{1}{3} \cdot W4 \quad W10 = 2.5 \cdot W12 \]

\[ W1 = 2 \cdot W4 \quad W6 = 2.5 \cdot W4 \]

\[ W8 = W12 \]
Comparison speed test bench
## Simulation Results Summary

<table>
<thead>
<tr>
<th>Supply</th>
<th>Temp.</th>
<th>Corner</th>
<th>Transition Time</th>
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<tbody>
<tr>
<td>4.5V</td>
<td>87°</td>
<td>SS</td>
<td>1.4520 ns</td>
</tr>
<tr>
<td>5.0V</td>
<td>27°</td>
<td>SF</td>
<td>0.8377 ns</td>
</tr>
<tr>
<td>5.0V</td>
<td>27°</td>
<td>TT</td>
<td>0.8317 ns</td>
</tr>
<tr>
<td>5.0V</td>
<td>27°</td>
<td>FS</td>
<td>0.8299 ns</td>
</tr>
<tr>
<td>5.5V</td>
<td>0°</td>
<td>FF</td>
<td>0.6045 ns</td>
</tr>
</tbody>
</table>
SS output
FF output
Test Bench Dynamic Offset
Dynamic Offset

Avg. dynamic offset = 6.49mV
Remaining things to do

• Add chicken DAC to vary the currents at the swing-minimizing circuit
• Overdrive recovery test bench
• Monte Carlo Analysis
• Layout
Conclusion

• All specifications met
• The first regeneration step (n-channel F-F) is very important, not only in increasing the speed, but in reducing the total input offset voltage. Layout with caution!