Comparator Design

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Outline

• Introduction
  - Architecture
  - Specifications
• Schematics
• Simulations
• Conclusion
ADC STAGE FOR 1.5b

Vin+
Vin-
Vref+
Vref-

A1
A2
B1
B2
CLK2

MSB
LSB
VDAC+
VDAC-

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>B1</th>
<th>B2</th>
<th>CLK2</th>
<th>MSB</th>
<th>LSB</th>
<th>VDAC+</th>
<th>VDAC-</th>
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</thead>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Vref-</td>
<td>Vref-</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>VDAC+</td>
<td>VDAC-</td>
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<tr>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>Vref+</td>
<td>Vref-</td>
</tr>
</tbody>
</table>

VDAC+
VDAC-
Output Waveforms of a Non-Overlapping Clock Generator.
Architecture & Specs

**SPECIFICATIONS**
- Offset < 100mV
- Decision time ≤ t_{nov}

**Regeneration**

Step 1: Phi2 getting low and Phi1 getting high.

Step 2: Phi1 gets high and M8 and M9 are closed.
Previous Comparator
Test bench for previous comparator
Layout Regenerative Nodes
TT OUTPUT
## Simulation Results

<table>
<thead>
<tr>
<th>CORNER</th>
<th>TEMP</th>
<th>SUPPLY</th>
<th>TRANSITION TIME (Ideal)</th>
<th>TRANSITION TIME W/ PARASITICS</th>
<th>NON-OVERLAP TIME</th>
<th>ZERO</th>
<th>ONE</th>
<th>TWO</th>
<th>THREE</th>
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<tbody>
<tr>
<td>SS</td>
<td>87°</td>
<td>4.5V</td>
<td>3.16ns</td>
<td>3.72ns</td>
<td>3.80ns</td>
<td>4.19ns</td>
<td>4.52ns</td>
<td>4.80ns</td>
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<tr>
<td>TT</td>
<td>27°</td>
<td>5.0V</td>
<td>1.62ns</td>
<td>2.08ns</td>
<td>2.50ns</td>
<td>2.80ns</td>
<td>3.0ns</td>
<td>3.20ns</td>
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</tr>
<tr>
<td>FF</td>
<td>0°</td>
<td>5.5V</td>
<td>1.22ns</td>
<td>1.29ns</td>
<td>1.80ns</td>
<td>2.06ns</td>
<td>2.22ns</td>
<td>2.40ns</td>
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Offset after Parasitic Extraction
Conclusion

• The specs are met on the final design.
• The offset on the comparator could be made better by balancing the regenerative nodes better on the layout.