Non-Overlapping Clock Generator.

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Outline.

- Introduction.
- Architecture 1.
- Architecture 2.
- Test Logic Implementation.
- Conclusion
Introduction.

The basic non-overlapping clock generator consists of a S-R flip-flop, with inverters in series before the feedback, to add delay as required.

Basic Non-Overlapping Clock Generator.
Introduction.

Output Waveforms of a Non-Overlapping Clock Generator.
Architecture 1.
Waveforms for \( \phi \) and \( \phi^- \) for conventional architecture.
Waveforms for phi and phi- for architecture1.
Delay Equations.

- Settling time ts.
  - For phi1 :- $T/2 - tr + t1 - t2 - t3 - t4 - t5 - t6 - t7 + tf.$
  - For phi2 :- $T/2 + tr - t1 - t2 - t3 - t4 - t5 - t6 - t7 - tf.$
- For lag :- $t6 + t7.$
- For $T_{nov}$: $t2 + t3 + t4.$
Architecture 1.

- This architecture, consist of a NAND gate at the output instead of the conventional NOT gate.
- The advantage of this is that it aligns the rising edges of both phi and phi-.
- The disadvantage of this kind of architecture is that the front end NAND gate does not contribute to non-overlapping time.
- Also, we need to size this NAND gate to drive a larger load.
Architecture 1.
Transistor level simulation waveforms for phi and phi-

Output waveforms for Architecture 1
Architecture 2.
Delay Equations.

- Settling time ts.
  - For phi1: $T/2 - tr + t1 - t2 - t3 - t4 - t5 - t6 - t7 + tf$.
  - For phi2: $T/2 + tr - t1 - t2 - t3 - t4 - t5 - t6 - t7 - tf$.

- For lag: $t6 + t7$.

- For Tnov: $t2 + t3 + t4 + t5 + t6 + t7$
Architecture 2.

- This represents the conventional non-overlapping clock generator.
- In this architecture the NAND gate at the input is followed by an inverter chain to achieve the required delay.
- Sizing of the Not gates to drive large load becomes easy as compared to architecture 1.
Architecture 2.
Transistor level simulation waveforms for phi and phi-

Output waveforms for Architecture 2
Test Logic.

- For implementing the test logic, we can add inverters in the feedback path.
- The delay can be provided by these inverters, which can be controlled by a multiplexer, whose select pin is brought outside the chip as a pin.
- Thus we can have multiple non-overlap times, to check the comparator circuit.
TEST LOGIC. behavioral model
Behavioral model waveforms for the test logic.

Delay select switch is flipped
**Conclusion.**

- The only advantage of Architecture 1 is that it provides aligned rise time between phi and phi-. This is offset by the inclusion of a NAND gate at the output, which makes driving large loads difficult also, the non-overlap time is less as compared to Architecture 2 for the number of gates used.

- Architecture 2 has non-aligned rise time between phi and phi-. It can drive larger load and also provide a larger non-overlap time for the number of gates used.