Non-Overlapping Clock Generator.

Kshitij Gujar
ADC2.
Outline.

• Introduction.
• Specifications.
• Schematics.
• Calculations/Trade-offs.
• Output waveforms.
• Floor plan.
Introduction.

• The basic non-overlapping clock generator consists of a S-R flip-flop, with inverters in series before the feedback, to add delay as required.
Introduction.

Output Waveforms of a Non-Overlapping Clock Generator.
Architecture
Delay Equations.

• Settling time ts.
  – For phi1 :- \( T/2 - tr + t1 - t2 - t3 - t4 - t5 - t6 - t7 + tf \).
  – For phi2 :- \( T/2 + tr - t1 - t2 - t3 - t4 - t5 - t6 - tf \).

• For lag :- \( t6 + t7 \).

• For Tnov :- \( t1 + t2 + t3 + t4 + t5 + t6 + \text{Delay} \)
NON-OVERLAPPING CLOCK GENERATOR

Company Name: CSUS

Title: NON-OVERLAPPING CLOCK GENERATOR
Project: PIPELINE PCC
Sheet: 4 of 16

Sheet: 1 of 1
Page: 1 of 1

Date: 4/16/2000
Time: 16:47
FEEDBACK DELAY
DELAY CHAINS

3.17ns

4ns

5.67ns

* INV SIZE-81/27, 18
Calculations.

• Calculation of load capacitance on the clock phases.
  – Load on each phase consists mainly of switches used in the Residue stage, Comparator and the Decode logic.
  – This obviously makes the load on each phase different.
  – Consideration also, has to be given for the capacitance introduced due to the routing of the clock.
Calculations.

- Load on phi1 phase.
  - Residue stage
    - 4 T-gates and 4 NMOS(3/0.6) switches.
      - Capacitance of each MOS is $W \times L \times Cox$
      - Capacitance of 4 NMOS switches 20fF (5fF each).
      - Capacitance of a single Tgate is 25fF
      - So the total capacitive load of the Residue stage on phase1 is 120fF/stage.
      - For seven pipe stages - 840fF.
  - Decode logic
    - Unit inverter(5.4/3,0.6)
      - Load of 12fF.
      - Total load on phi1 - 1.022pF*
Calculations.

• Load on phi2 phase.
  – Residue stage
    • 2 T-gates and 4 NMOS(3/0.6) switches.
    → Capacitance of each MOS is \( W \times L \times Cox \)
    → Capacitance of 4 NMOS switches 20fF (5fF each).
    → Capacitance of a single Tgate is 25fF
    So the total capacitive load of the Residue stage on phase2 is 130fF/stage.
    → For seven pipe stages-910fF.
  – Decode logic
    • Unit inverter(5.4/3,0.6)
    → Load of 12fF.
    Total load on phi1- 1.12pF*
Calculations.

- **Load on phi1- phase.**
  - **Residue stage**
    - 2 NMOS switches (3/0.6).
    - Capacitance of each MOS is $W \times L \times Cox$.
    - So the total capacitive load of the Residue stage on phase1- - is 10 fF/stage.
    - For seven pipe stages-70fF.
  - **Comparator**
    - 1 Inverter (9/3,0.6) and 1 NMOS (3/0.6) switch.
    - Total capacitive load is 25fF/stage

- **So total load on phase phi1- is 450fF*.**
Calculations.

• Load on phi2- phase.
  – Comparator
    • 2 NAND gates(9/3,0.6).
      → Total capacitive load is 40fF/stage.
  
• So total load on phase phi2- is 480fF*.
Calculations.

• Routing capacitance.
  – The required length of routing for the clocks is about 1700 u. This value was derived from the overall floor plan.
  – While calculating the routing capacitance we have to take into account the fringe to substrate capacitance and the substrate capacitance to metal.
  – All the clock routing will be done using METAL 3.
Calculations.

• Routing capacitance (contd.)
  – Fringe capacitance value for AMI 0.5u process is 39.8aF/u
  – Substrate capacitance value for the process is 10.8aF/sq.
  – The METAL 3 line width is kept as 2u.
  – This yields a total routing parasitic of 0.2pF.
Calculations.

- Calculation of the bond wire inductance and the total equivalent package inductance at VDD and GND pins.
  - The main aim in this case is to keep the equivalent package inductance minimum.
  - This can be achieved by using pins that have bond fingers near to the outer pins.
Typical Corner Tnov.

24-Apr-2004  File: schematic_mux_inv_tb_eldonet.com
00:56:53  CORNER-TT, Tnov-4ns, (TEST MODE 42)
Fast-Fast Corner (minimum Tnov)

24-Apr-2004  File: schematic_mux_inv_th_eldonet.com
01:54:26  CORNER-FF, SUPPLY-5.5V, TEMP-0, Tnov-1.09ns, (TEST NODE-0)
GROUND Bounce.

24-Apr-2004  File: schematic_mux_inv_tb_eldonet.cou
00:19:01  CORNER-FF, SUPPLY-5.5V, TEMP-0°C, Tnov-1.09ns (TEST MODE 0)
Tlag.
Trise.

24-apr-2004 File: schematic_mux_inv_th_eldonet.cou
02:17:19 ELDO v6.3_1.1 (Production version) : CORNER-FS, Trise-0.27ns
### Tnov 1.6ns (over all corners)

<table>
<thead>
<tr>
<th>in ns</th>
<th>TR</th>
<th>TF</th>
<th>Period</th>
<th>TR</th>
<th>TF</th>
<th>Period</th>
<th>TR</th>
<th>TF</th>
<th>T lag</th>
<th>TR</th>
<th>TF</th>
<th>Tlag</th>
<th>Tnov</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tnov 1.6ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TT</td>
<td>0.27</td>
<td>0.27</td>
<td>23.29</td>
<td>0.27</td>
<td>0.27</td>
<td>23.35</td>
<td>0.3</td>
<td>0.3</td>
<td>0.2</td>
<td>0.3</td>
<td>0.3</td>
<td>0.19</td>
<td>1.67</td>
</tr>
<tr>
<td>FS</td>
<td>0.28</td>
<td>0.26</td>
<td>23.29</td>
<td>0.28</td>
<td>0.26</td>
<td>23.33</td>
<td>0.31</td>
<td>0.3</td>
<td>0.2</td>
<td>0.31</td>
<td>0.3</td>
<td>0.2</td>
<td>1.68</td>
</tr>
<tr>
<td>SF</td>
<td>0.26</td>
<td>0.28</td>
<td>23.28</td>
<td>0.26</td>
<td>0.26</td>
<td>23.36</td>
<td>0.28</td>
<td>0.31</td>
<td>0.2</td>
<td>0.31</td>
<td>0.3</td>
<td>0.19</td>
<td>1.67</td>
</tr>
<tr>
<td>FF</td>
<td>0.2</td>
<td>0.21</td>
<td>23.82</td>
<td>0.2</td>
<td>0.21</td>
<td>23.98</td>
<td>0.23</td>
<td>0.23</td>
<td>0.14</td>
<td>0.22</td>
<td>0.24</td>
<td>0.13</td>
<td>1.09</td>
</tr>
<tr>
<td>SS</td>
<td>0.38</td>
<td>0.4</td>
<td>22.16</td>
<td>0.38</td>
<td>0.4</td>
<td>22.01</td>
<td>0.43</td>
<td>0.45</td>
<td>0.33</td>
<td>0.43</td>
<td>0.45</td>
<td>0.33</td>
<td>2.9</td>
</tr>
</tbody>
</table>
**Tnov 3.1ns (over all corners)**

<table>
<thead>
<tr>
<th>in ns</th>
<th>TR</th>
<th>TF</th>
<th>Period</th>
<th>TR</th>
<th>TF</th>
<th>Period</th>
<th>TR</th>
<th>TF</th>
<th>Tlag</th>
<th>TR</th>
<th>TF</th>
<th>Tlag</th>
<th>Tnov</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Tnov 3.1ns</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>TT</strong></td>
<td>0.25</td>
<td>0.28</td>
<td>21.8</td>
<td>0.25</td>
<td>0.28</td>
<td>21.86</td>
<td>0.28</td>
<td>0.31</td>
<td>0.19</td>
<td>0.28</td>
<td>0.31</td>
<td>0.2</td>
<td>3.16</td>
</tr>
<tr>
<td><strong>FS</strong></td>
<td>0.26</td>
<td>0.27</td>
<td>21.78</td>
<td>0.26</td>
<td>0.27</td>
<td>21.83</td>
<td>0.29</td>
<td>0.3</td>
<td>0.2</td>
<td>0.28</td>
<td>0.31</td>
<td>0.2</td>
<td>3.19</td>
</tr>
<tr>
<td><strong>SF</strong></td>
<td>0.23</td>
<td>0.28</td>
<td>21.83</td>
<td>0.23</td>
<td>0.28</td>
<td>21.9</td>
<td>0.27</td>
<td>0.31</td>
<td>0.2</td>
<td>0.26</td>
<td>0.31</td>
<td>0.19</td>
<td>3.13</td>
</tr>
<tr>
<td><strong>FF</strong></td>
<td>0.19</td>
<td>0.22</td>
<td>22.76</td>
<td>0.19</td>
<td>0.22</td>
<td>22.92</td>
<td>0.22</td>
<td>0.24</td>
<td>0.14</td>
<td>0.22</td>
<td>0.24</td>
<td>0.13</td>
<td>2.15</td>
</tr>
<tr>
<td><strong>SS</strong></td>
<td>0.36</td>
<td>0.4</td>
<td>19.84</td>
<td>0.37</td>
<td>0.39</td>
<td>19.69</td>
<td>0.4</td>
<td>0.45</td>
<td>0.33</td>
<td>0.42</td>
<td>0.46</td>
<td>0.33</td>
<td>5.22</td>
</tr>
</tbody>
</table>
## Tnov 4ns (over all corners)

<table>
<thead>
<tr>
<th></th>
<th>PHI1 TR</th>
<th>PHI1 TF</th>
<th>PHI1 Period</th>
<th>PHI2 TR</th>
<th>PHI2 TF</th>
<th>PHI2 Period</th>
<th>PHI1- TR</th>
<th>PHI1- TF</th>
<th>PHI1- Tlag</th>
<th>PHI2- TR</th>
<th>PHI2- TF</th>
<th>PHI2- Tlag</th>
<th>Tnov</th>
</tr>
</thead>
<tbody>
<tr>
<td>in ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tnov 4ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TT</td>
<td>0.24</td>
<td>0.28</td>
<td>20.95</td>
<td>0.24</td>
<td>0.28</td>
<td>21.01</td>
<td>0.26</td>
<td>0.31</td>
<td>0.19</td>
<td>0.25</td>
<td>0.31</td>
<td>0.2</td>
<td>4.02</td>
</tr>
<tr>
<td>FS</td>
<td>0.25</td>
<td>0.27</td>
<td>20.9</td>
<td>0.25</td>
<td>0.27</td>
<td>20.96</td>
<td>0.26</td>
<td>0.3</td>
<td>0.2</td>
<td>0.26</td>
<td>0.31</td>
<td>0.2</td>
<td>4.06</td>
</tr>
<tr>
<td>SF</td>
<td>0.23</td>
<td>0.28</td>
<td>20.97</td>
<td>0.23</td>
<td>0.28</td>
<td>21.05</td>
<td>0.25</td>
<td>0.32</td>
<td>0.19</td>
<td>0.25</td>
<td>0.31</td>
<td>0.19</td>
<td>3.98</td>
</tr>
<tr>
<td>FF</td>
<td>0.18</td>
<td>0.22</td>
<td>22.14</td>
<td>0.19</td>
<td>0.22</td>
<td>22.3</td>
<td>0.21</td>
<td>0.24</td>
<td>0.14</td>
<td>0.2</td>
<td>0.24</td>
<td>0.13</td>
<td>2.77</td>
</tr>
<tr>
<td>SS</td>
<td>0.37</td>
<td>0.4</td>
<td>18.5</td>
<td>0.37</td>
<td>0.39</td>
<td>18.35</td>
<td>0.39</td>
<td>0.45</td>
<td>0.33</td>
<td>0.39</td>
<td>0.46</td>
<td>0.33</td>
<td>6.56</td>
</tr>
</tbody>
</table>
Tnov 5.6ns (over all corners)

<table>
<thead>
<tr>
<th></th>
<th>PHI1</th>
<th></th>
<th>PHI2</th>
<th></th>
<th>PHI1-</th>
<th></th>
<th>PHI2-</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TR</td>
<td>TF</td>
<td>Period</td>
<td>TR</td>
<td>TF</td>
<td>Period</td>
<td>TR</td>
<td>TF</td>
</tr>
<tr>
<td>in ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tnov 5.6ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TT</td>
<td>0.23</td>
<td>0.26</td>
<td>19.28</td>
<td>0.23</td>
<td>0.28</td>
<td>19.33</td>
<td>0.25</td>
<td>0.31</td>
</tr>
<tr>
<td>FS</td>
<td>0.24</td>
<td>0.27</td>
<td>19.21</td>
<td>0.24</td>
<td>0.27</td>
<td>19.25</td>
<td>0.25</td>
<td>0.3</td>
</tr>
<tr>
<td>SF</td>
<td>0.22</td>
<td>0.28</td>
<td>19.33</td>
<td>0.22</td>
<td>0.28</td>
<td>19.41</td>
<td>0.25</td>
<td>0.31</td>
</tr>
<tr>
<td>FF</td>
<td>0.17</td>
<td>0.22</td>
<td>20.93</td>
<td>0.17</td>
<td>0.22</td>
<td>21.08</td>
<td>0.2</td>
<td>0.24</td>
</tr>
<tr>
<td>SS</td>
<td>0.37</td>
<td>0.4</td>
<td>15.83</td>
<td>0.36</td>
<td>0.39</td>
<td>15.68</td>
<td>0.39</td>
<td>0.46</td>
</tr>
</tbody>
</table>
THINGS TO DO!

• Re-adjust the size of the output buffers to meet the changes load specs (if any).

• Figure out the chip area required.