Architecture Review

Residue Stage
(Sub-DAC, S/W capacitor circuit and op amp)

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Introduction

- General block diagram of a pipelined A/D

Each pipeline stage
- Samples and holds analog input
- Sub-ADC generates digital output
- DAC & s/w cap yield quantization error
- Quantization error is restored
Understanding residue stage

Sub-DaC : Accepts digital output from the ADC and converts to \(V_{\text{ref}+}, 0\) or \(V_{\text{ref}-}\).

S/W capacitor and op-amp: sample the input signal and then amplify by 2 and subtract from the DAC output voltage to generate residue.
Architecture selection: DAC

- **R-DAC**: Resistor DAC
  - R values must be small
  - Consumes a lot of power
  - Mismatching of individual Res. Due to process gradient

- **C-DAC**: Capacitor DAC
  - Consumes less power
  - Capacitor matching is critical
  - Calibration techniques have to be used.
The selected DAC architecture

- A1, B1, A2 and B2 are the outputs of the two fully differential comparators. (A2 = A1 ! And B2 = B1 !)
- DAC supplies voltage to gain stage as well as digital word to DCL.
DAC contd.

- **DAC output Values:**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>B1</th>
<th>B2</th>
<th>φ₂</th>
<th>MSB</th>
<th>LSB</th>
<th>V_{dac1}</th>
<th>V_{dac2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>V_{ref}</td>
<td>V_{ref}</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>V_{dac2}</td>
<td>V_{dac1}</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>V^{+}_{ref}</td>
<td>V^{-}_{ref}</td>
</tr>
</tbody>
</table>

- **Understanding:**
  If the $V_i$ (actual input) is $< -V_{ref}/4$, then comparator outputs are 0 0 and the DAC converts the voltage to $-V_{REF}$ as required.

- **Similarly other cases**
DAC architecture optimized

Implementation using T-Gates:

- Advantages:
  - Cancellation of channel-charge
  - Fairly constant switch resistance.
S/W capacitor circuit

- A fully differential S/W capacitor circuit:
S/W capacitor circuit contd.

- **Sampling phase**

\[ V_s = \begin{cases} 
(1 + \frac{C_s}{C_f})V_i - V_{ref}, & \text{if } V_i > V_{ref}/4 \\
(1 + \frac{C_s}{C_f})V_i, & \text{if } -V_{ref}/4 \leq V_i \leq +V_{ref}/4 \\
(1 + \frac{C_s}{C_f})V_i + V_{ref}, & \text{if } V_i < -V_{ref}/4 
\end{cases} \]

- **Amplification phase**
Conclusion

- Architectures for the Sub-DAC and S/W capacitors have been analyzed in detail.
- Some minor changes are possible during the design phase.
- Problems associated are avoided using advanced clocking and T gate implementation.
References

- Design for reliability of low voltage, s/w capacitor – by Andrew Abo
- UMaine Kannan Sockalingam & Rick Thibodeau