Design Review
Residue Stage Op Amp

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Overview

• Introduction
• Specifications
• Design of the Op Amp
• Calculations for the W and L sizes.
• Offset calculation
• Simulation Results over corners
• Switched capacitor CMFB (Design and Simulations)
Introduction

• Basic op amp requirements:
  High gain
  High bandwidth
• Architectural considerations:
  Two stage op amp
  Folded cascode op amp
  Telescopic op amp
Architecture Recap

- The selected architecture
- Limited output swing
- High gain
- High bandwidth
Specifications Required

- Gain $\geq 80\text{db}$
- Bandwidth $\geq 250\text{Mhz}$
- Phase Margin (when $\beta=1/4$) $= 65-70\text{degrees}$.
- Offset Value $\leq 10\text{mv}$
- Settling time $\leq 18\text{ns}$.

Designed op amp needs to meet all the above requirements.
Initial Design
Initial Design: Issues

• The gain of the circuit was found to be lower than the required specification.
• The phase and bandwidth were also barely meeting spec.
• Solutions:-
  • Redesign
  • Add an additional cascode device.
Sizing calculations for the op amp (initial)

Equations and values used:

\[ \text{Id} = \frac{\mu_n \text{Cox} (w/L)}{2} \times (V_{on})^2 \]
\[ \mu_n \text{Cox} = 114 \quad \text{and} \quad \mu_p \text{Cox} = 53 \]
\[ V_{tn} = 0.8 \quad V_{tp} = 0.9 \]
\[ \text{Bandwidth} = \frac{g_m}{C_L} \]
\[ C_L = 1.25 \text{pF} \]
\[ G_m = \frac{2 \times \text{Id}}{V_{on}} \]
\[ \text{Rout} = \frac{1}{\lambda \times \text{Id}} \]

- **Input devices:**
  - \( \text{Id} = 500 \mu A \)
  - \( V_{on} = 0.25V \)
  - \( W/L = 100u/0.75u \)

- **Pmos Load:**
  - \( \text{Id} = 500 \mu A \)
  - \( V_{on} = 0.4V \)
  - \( W/L = 180u/1.5u \)

- **Tail Current Mirror:**
  - \( \text{Id} = 1050 \mu A \)
  - \( V_{on} = 0.4V \)
  - \( W/L = 120u/1u \)

- **Biasing device:**
  - \( \text{Id} = 50 \mu A \)
  - \( V_{on} = 2V_{on(nmos)} + V_t(0.8) \)
  - \( W/L = 3u/0.6u \)
Proposed Design
Bias current Network

- The input bias current = 75 µA
- Ratio of devices 1:5 and hence mirrored current = 375 µA.
Pmos wide swing current mirror and load

- A ratio of $1/8$ between for the wide swing mirror
Input Devices

- Sized the second cascode lower to increase the bandwidth
- First cascode device was sized to get the required phase margin
- Input devices were sized bigger to increase gm and hence the gain
<table>
<thead>
<tr>
<th>I/P devices</th>
<th>Calculated</th>
<th>W/L</th>
<th>Von (mV)</th>
<th>Id (µA)</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>100/0.75</td>
<td>250</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td>Final</td>
<td>320/0.75</td>
<td>180</td>
<td>375</td>
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<tr>
<td>Pmos Load</td>
<td>Calculated</td>
<td>180/1.5</td>
<td>400</td>
<td>500</td>
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<tr>
<td></td>
<td>Final</td>
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<tr>
<td>Tail current</td>
<td>Calculated</td>
<td>120</td>
<td>400</td>
<td>1100</td>
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<tr>
<td></td>
<td>Final</td>
<td>200</td>
<td>350</td>
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Simulation at SS 85degree 4.5V

Gain and phase plot
Simulation result Low Supply=4.5V and high Temperature=85

<table>
<thead>
<tr>
<th>Desired Values</th>
<th>Gain</th>
<th>UGBW</th>
<th>Phase (at12d)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>&gt;80db</td>
<td>&gt;250Mhz</td>
<td>70°-75°</td>
</tr>
<tr>
<td>SS</td>
<td>85db</td>
<td>257Mhz</td>
<td>70</td>
</tr>
<tr>
<td>FF</td>
<td>83db</td>
<td>316Mhz</td>
<td>72</td>
</tr>
<tr>
<td>SF</td>
<td>84db</td>
<td>280Mhz</td>
<td>72</td>
</tr>
<tr>
<td>FS</td>
<td>85db</td>
<td>290Mhz</td>
<td>71</td>
</tr>
<tr>
<td>TT</td>
<td>85db</td>
<td>267Mhz</td>
<td>71</td>
</tr>
</tbody>
</table>
Simulation at room temp and full supply voltage

Gain and Phase Plot
Simulation results at Temp=27 and supply voltage=5V

<table>
<thead>
<tr>
<th>Desired Values</th>
<th>Gain</th>
<th>UGBW</th>
<th>Phase (at12d)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Desired Values</td>
<td>&gt;80db</td>
<td>&gt;250Mhz</td>
<td>70°-75°</td>
</tr>
<tr>
<td>SS</td>
<td>88db</td>
<td>290Mhz</td>
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<tr>
<td>FF</td>
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<tr>
<td>TT</td>
<td>87db</td>
<td>327Mhz</td>
<td>70</td>
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</table>
Switched Capacitor CMFB

- Design Considerations:
  - The switch sizes can be minimum
  - The capacitors being switched can be between one-quarter to one-tenth of non-switched capacitors.
  - Cannot be too big as they might add extra load to the op amp during phase 2 and cannot be too small.
Designed S/W cap CMFB ckt.
CMFB calculations

- To ensure the stability and reasonable settling of the common mode feedback, the bandwidth can be 50% of the unity gain bandwidth.

\[
\frac{2C_{cm}}{2C_{cm} + C_{gs10}} \geq 50\% \times F \omega_u
\]

\[
\Rightarrow C_{cm} = \frac{F \omega_u \times CL \times C_{gs10}}{2(1 - F \omega_u CL)}
\]

The calculated value of Ccm was found to be 50fF, and hence the values greater than 50fF would give us the stability required and settling time.
Floor plan for the op-amp

Quiet Routing channel

- Vdd
- Pmos Current sources and cascodes
- Nmos Diff pair and cascodes
- Nmos Current sources and cascodes
- Vss
- Dedicated shielded well for the inputs
Issues faced and solutions

• Issues found when integrated with the residue stage s/w cap circuit.
• High Overshoot
• Solutions done
• Adjust the size of the cascode device for a higher phase margin.
Conclusions

• The designed op amp meets the specifications.

• Future considerations:-
  – Design issues to be resolved before layout.
  – Optimize design
  – CMFB stability check
Appendix

- Offset Calculations
- $\text{Avtn}=10.71$  $\text{Avtp}=17.8$  $\beta_n=.1\%$  $\beta_n=.2\%$
- $\sigma_{vtn}(1,2)=1.26\text{mv}$  $\sigma_{vtn}(3,4)=1.26\text{mv}$
- $\sigma_{vtp}(1,2)=1.21\text{mv}$
- $\sigma_{Vos}=2.2\text{mv}$ and hence $3\sigma=6.8\text{mv} \leq 10\text{mV}$ (meets specifications)
- The final devices used are bigger in size and hence will have lower value of offset