Digital decode & Error Correction for 8 bit pipelined ADC employing 1.5bit/stage

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Outline

• Introduction
• Need for digital decode & Error Correction
• Different architectures for digital decode & Error correction
• Implementation
• Conclusion
Introduction

Pipelined ADC overview
Need for digital decode

• To eliminate the redundancy of $\frac{1}{2}$ bit in each stage
• Digital correction is included in order to avoid additive noise created by simultaneously driving high–speed digital signals during the conversion operation.
• Digital correction takes raw output data of the ADC as input and outputs the digital representation.
• Digital circuits are fast and take low power.
How is it done

Requirements:

- Align ADC (comparator) decisions
- Correct ADC output bit pattern
- Add digital data in a 1.5-bit fashion
- Output a 8-bit digital word
Different architectures to get 8 bit output

- Align ADC decisions
  Shift Register (Delayed D flip-flop)

- Addition of digital data
  I. Ripple carry Adder
  II. Carry look ahead Adder
Shift register to align ADC decisions

Shift register using D flipflop
Digital correction logic

Concept of Digital Correction

STAGE - 1

STAGE - 2

STAGE - 3

STAGE - 4

STAGE - 5

STAGE - 6

STAGE - 7

Z = D
Y = B XOR C
X = A + BC (CARRY BIT)

Mathematical analysis Of Digital Correction
Logic Equations used for RCA

- Total gate delay for RCA

\[
\begin{align*}
D_0 &= B_1 \\
C_0 &= A_2 + A_1B_2 & D_1 &= A_1 \oplus B_2 \\
C_1 &= B_3C_0 + A_3 & D_2 &= C_0 \oplus B_3 \\
C_2 &= B_4C_1 + A_4 & D_3 &= C_1 \oplus B_4 \\
C_3 &= B_5C_2 + A_5 & D_4 &= C_2 \oplus B_5 \\
C_4 &= B_6C_3 + A_6 & D_5 &= C_3 \oplus B_6 \\
& & D_6 &= C_4 \oplus B_7 \\
& & D_7 &= B_7C_4 + A_7
\end{align*}
\]
Ripple Carry Adder

\[ A + BC \]
Simulation Result for Ripple Carry Adder

- Simulated AND-OR gate
- Number of stages = 6
  Total delay = 6 * Delay of one AND- OR gate
- Typical simulation and Worst case values observed

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<tbody>
<tr>
<td>TT</td>
<td>27°C</td>
<td>5 V</td>
<td>0.5ns</td>
<td>3ns</td>
</tr>
<tr>
<td>SS</td>
<td>85°C</td>
<td>4.5 V</td>
<td>0.5ns</td>
<td>3ns</td>
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- Total gate delay is < 25 ns (half the clock cycle period)
Carry Look Ahead Adder

• Advantages over RCA
  ▪ Used to avoid delay associated with the “Rippling” of the carry bits in RCA
  ▪ Faster than Ripple carry adder

• Takes more area and power
Conclusion

• 6 stages of ripple carry adder take 3ns delay in worst case.

• Ripple carry adder meets the desired delay of 25ns (half the clock period). Thus seems to be suitable choice for the architecture.