Architecture Review
Comparator

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OUTLINE

• Basic function of Comparator
• Topology 1
• Problems with other Topologies
• Topology 2 (under consideration)
• Advantages of this topology
• Simulation and its results
• Conclusion
• References
Comparator

• Fully differential to eliminate the effect of noise
• Offset voltage tolerance up to $\pm V_{\text{ref}}/4$
• Two comparators in each stage except in last stage
• Three comparators in last stage
Basic Function of Comparator

• Being the part of Sub-ADC the basic function of comparator is to take analog value as i/p and give digital value as o/p

<table>
<thead>
<tr>
<th>I/P values</th>
<th>MSB (Comp1)</th>
<th>LSB (Comp0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vin &lt; -Vref/4</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>-Vref/4 &lt; Vin &lt; Vref/4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Vin &gt; Vref/4</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Fig. 10. Differential comparator.

\[ V_o = V_i - V_{\text{ref}}/4 \]
Topology 1 cntd.

Fig. 11. Comparator preamp and latch.
Problems with Topology 1

• Problems
  – Capacitor mismatch
  – Dependent on two clocks
  – More Area
  – High settling time
Differential Pair Latching Comparator
Differential Pair Latching Comparator

• Advantages
  – Mismatch insensitive
  – Only a single phase clock
  – $\pm\text{V}_{\text{ref}}/4$ as direct inputs to comparator. Hence, no need of any extra capacitor or resistor network as obtained from Reference voltage generator guy.
Simulation and its Results
Waveforms
Simulation of ClkRSLatch
Waveforms (latch and Clock in phase)
Waveforms (latch and Clock out of phase)
Issues to be Resolved

- Time taken for conversion
- Size of Transistors
- Clock to RS latch should in phase or out of phase with the Latch signal to comparator
• CONCLUSION
  – Topology 2 more appropriate for us
  – Still to consider time taken for conversion
  – Still to consider device sizes
References

• A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter - Lauri Sumanen, Student Member, IEEE, Mikko Waltari, Student Member, IEEE, and Kari A. I. Halonen

• A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter - Andrew M. Abo and Paul R. Gray, Fellow, IEEE