Final Design Review
Comparator

BY
CHINTAN VIBHAKAR
OUTLINE

• Comparator Basic Function
• Architecture
• Sims w/o Parasitics
• Sims with Parasitics
• Comparison
• Complete Design sims with Parasitics
• Conclusion
Comparator Basics

I/P  PVREFby4  NVREFby4

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>B1</th>
<th>MSB</th>
<th>LSB</th>
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<tbody>
<tr>
<td>I/P &lt; -0.25</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<tr>
<td>-0.25&lt; I/P&lt;0.25</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td>I/P &gt; 0.25</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
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</table>

A1 – Upper Comp P Out
B1 – Lower Comp P Out
-A1, B1 given to sub-DAC
-MSB & LSB given to Digital Decode
TEST BENCH FOR
SIMULATION
Comparators making decision on negedge of P1 adv
Settling Time = 2.47 ns
LOCK OUT ON POSEDGE OF P2 adv
SIMS With Parasitics
Comparators making decision on negedge of P1 adv

Comparators making decision on negedge of P1 adv
Settling Time = 2.55 ns
LOCK OUT ON POSEDGE OF P2 adv
## COMPARISION
SIMS RESULTS FOR DIFFERENT CORNERS
WITH and W/O PARASITICS

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<th>5.5V</th>
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<td>0°C</td>
<td>27°C</td>
<td>85°C</td>
<td>0°C</td>
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<td>85°C</td>
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Note: All dimensions are in ns
TOP LEVEL COMPARATOR

[Diagram of a comparator circuit with labels for VDD, VIN, VREFP, VREFN, VIP, GND, PHI1, PHI2, MSB, LSB, A1, A2, B1, B2, etc.]

[Note: The diagram shows the electrical connections and signals.]
SIMS FOR TOP LEVEL COMPARATOR

I/P > 0.25 V
Hence, A1 = 1, B1 = 1

I/P < -0.25 V
Hence, A1 = 0, B1 = 0
Comp making decision

-0.25 V < I/P < 0.25 V

Hence,
A1 = 0
B1 = 1

I/P < -0.25 V

Hence,
A1 = 0
B1 = 0

I/P > 0.25 V

Hence,
A1 = 1
B1 = 1
-0.25 V < I/P < 0.25 V
Hence,
A1 = 0     B1 = 1
MSB = 0     LSB = 1

I/P > 0.25 V
Hence,
A1 = 1     B1 = 1
MSB = 1     LSB = 0

I/P < -0.25 V
Hence,
A1 = 0     B1 = 0
MSB = 0     LSB = 0
Conclusion

• My design meets all the specification with the Parasitics.
THANK YOU
Corner Case 2 (1mv Diff w/o para)
Corner Case 2 (1mv Diff with para)