Including Testpoints and Teardrops on the PCB

Printed circuit board testpoints are locations on the board that can be used to test the correct function of the board. Testpoints are used to validate the board before the components are added – ensuring that the connectivity and isolation requirements of the routing is correct, and after the board is assembled – ensuring that the circuit functions within the design specifications.

Each testpoint is a location where a test probe can be connected to the PCB. Test probes can be connected by automated test equipment (typically by a bed-of-nails type test jig), or they can be connected by a person during manual testing.

The automated test equipment applies voltages and currents to each testpoint in turn, and simultaneously takes measurements at the other testpoints. On an unloaded board the PCB can be tested for correct continuity between every node in each net, for shorts between different nets, and the isolation resistance between nets can be measured. On an assembled board the testpoints are used to measure the performance of the circuit.

The steps you go through to add testpoints to your design include:

- Defining what is a valid testpoint
- Defining which nets require testpoints
- Finding existing pads and vias that can be used as testpoints
- Adding testpoints during the autorouting process
- Reporting the location of each testpoint
- Reporting any nets that failed to receive a testpoint

What is a Testpoint?

Both pads and vias can be used as testpoints, by enabling one or both of their testpoint attributes. These attributes allow any pad or via to be nominated as a top layer testpoint, a bottom layer testpoint, or as a top layer and bottom layer testpoint.

Keep the testing method in mind when you choose the side of the board that testpoints will be allowed on – will the board be probed from the bottom side only, or the top side only, do some points need to be on the bottom for automated testing and others on the top for infield testing, and so on.

Defining the properties of pads and vias that can be used as Testpoints is done by configuring the Testpoint Style design rule.
The testpoint style design rule defines the properties of the pads/vias that can be used as testpoints.

The Testpoint Style design rule specifies the allowable physical parameters of pads and vias that are used as testpoints. The attributes of the rule include:

**Allow testpoint under component** – If this option is enabled testpoints are allowed under a component, on the same side of the board that the component is mounted on. Testpoints that are under a component, but on the opposite side of the board, are always permitted. Normally the only time you would allow a testpoint under a component would be when that testpoint is used for testing the board prior to assembly.

**Style** – The Min and Max settings define the minimum and maximum pad/via diameter and hole diameter of a valid testpoint. These settings are used by the Testpoint Find feature, and by the on-line and batch DRC. The Preferred settings define the size of testpoint pads placed by the autorouter. Set the Style settings to suit your testpoint requirements.

**Allowed Side** – These options define the side of the board the testpoint must be on, and whether the testpoint can be pads/vias with a hole, or single-sided pads. These settings are used as preferences by the Testpoint Find feature when it searches for possible
testpoints, and by the Autorouter when it places testpoints. The Testpoint Find feature and the Autorouter use the options in the following pre-defined order:

- Bottom – bottom layer surface mount pad
- Top – top layer surface mount pad
- Bottom thru-hole – bottom side of a via
- Top thru-hole – top side of a via
- Bottom thru-hole – bottom side of a pad with a hole
- Top thru-hole – top side of a pad with a hole

Each setting is only considered if it is enabled. The bottom thru-hole option enables both bottom side thru-hole pads and vias (and likewise for the top thru-hole option) – they are listed separately to show that vias have a higher priority during testpoint searching by the Testpoint Find feature.

**Grid Size** – The grid is used by the Testpoint Find feature when it attempts to locate possible testpoint sites.

**Testpoint Usage Design Rule**

This rule is used to specify which nets must have a testpoint, or which nets must not have a testpoint. Set the rule scope to target those nets that must have a testpoint.

**Locating Existing Testpoint Sites**

The Testpoint Find feature searches for existing pads and vias that can be used as testpoints. Select **Tools » Find and Set Testpoints** from the menus to run the Testpoint Find feature. Obeying the Testpoint Usage and Testpoint Style rules, this feature will analyze the PCB and attempt to find a pad or via that complies with the Testpoint Style rule, for each net covered by the Testpoint Usage design rule, and set the appropriate testpoint attribute for that pad or via. When it has finished, a dialog will appear reporting how many pads and vias were found and set to testpoints (found testpoints are left selected once it has finished). All Testpoint attributes can be cleared at any time by selecting **Tools » Clear all Testpoints** from the menus.

If the pre-defined Allowed Side order is not appropriate for your design when you are using the Testpoint finder, run multiple passes with different allowed side settings.

**Adding Testpoints with the Autorouter**

Enable the Add Testpoints option in the Autorouter Setup dialog to instruct the autorouter to attempt to add testpoints once it completes all other routing passes, in accordance with the Testpoint Style and Testpoint Usage design rules.

If the Add Testpoints option is enabled the autorouter first scans the board for possible existing testpoint pads/vias, then attempts to place a testpoint pad in each net which still needs one.
Reporting the Location of Each Testpoint

The CAM Manager testpoint report includes complete details about each testpoint on the board. Select File » CAM Manager from the menus to create a new CAM document, where you can set up a Testpoint report. Refer to the chapter, Generating the Manufacturing Files, for complete details on using the CAM Manager to generate a Testpoint report.

Reporting Nets that Failed to Receive a Testpoint

The DRC report can list each net that failed to receive a testpoint in accordance with the Testpoint design rules. Enable the Testpoint Usage rule on the Report Tab of the Design Rule Check dialog (select Tools » Design Rule Check), enable the Create Report File option at the bottom of the dialog, then click the Run DRC button at the bottom of the dialog to generate the report. The report will include a list of nets that do not include a testpoint.

Enable the Testpoint Style rule in the Design Rule Check dialog to ensure that the pads and vias that are flagged as testpoints fit within the requirements of the Testpoint Style design rule.

Clearing all Testpoints from the Board

The Testpoint attribute for all pads and vias can be cleared at any time by selecting Tools » Clear all Testpoints from the menus.

Adding Teardrops to Pads and Vias

Teardrops can be added to pads and vias by selecting Tools » Teardrops from the menus. This will pop up the Teardrop Options dialog, where you configure the teardrop requirements. The dialog includes the following options.

All Pads – Add teardrops to all pads, in accordance with the Selected Objects Only and Force Teardrops options.

All Vias – Add teardrops to all vias, in accordance with the Selected Objects Only and Force Teardrops options.

Selected Objects Only – Add Teardrops to selected pads and vias only. Use this option when you need to teardrop some pads/vias, but not others. Use the global editing feature to change the selection status of the pads/vias that need to have teardrops.

Force Teardrops – Place teardrops on all pads/vias, including those where the teardrop tracks/arches will create a DRC violation.

Create Report – Create a report file which lists the number of pads and vias that teardropping was attempted on, as well as each pad and via that was not teardropped, or not completely teardropped.