Instruction: 

Address: CS : 

Operation: 

Dest.: 

Source: 

Instruction Format

Binary: 

Hex: 

Instruction: 

Address: CS : 

Operation: 

Dest.: 

Source: 

Instruction Format

Binary: 

Hex: 

Instruction: 

Address: CS : 

Operation: 

Dest.: 

Source: 

Instruction Format

Binary: 

Hex: 

Instruction: 

Address: CS : 

Operation: 

Dest.: 

Source: 

Instruction Format

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Instruction: 

Address: CS : 

Operation: 

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Source: 

Instruction Format

Binary: 

Hex:
Example

Instruction: Mov DL, 25

Address: CS:0100 Operation: Mov Dest.: DL Source: 25
immediate to register (alternate encoding)

Instruction Format: 1011 w reg : immediate data
w=0 reg DL=010 data=0010 0101
Binary: 1011 0010 0010 0101
Hex: B2 25

Instruction: Mov BL, [0200]

Address: CS:0102 Operation: Mov Dest.: BL Source: [0200]
memory to reg

Instruction Format: 1000 1010 0001 1110 r/m=110 memory address = 0002
Binary: 1000 1010 0001 1110 0000 0000 0000 0010
Hex: 8A 1E 00 02

Instruction: ADD BL, DL

Address: CS:0106 Operation: ADD Dest.: BL Source: DL, BL
register2 to register1

Instruction Format: 0000 001w : 11 reg1 reg2
w=0 reg1=BL=011 reg2=DL=010
Binary: 0000 0010 1101 1010
Hex: 02 DA

Instruction: INT 20

Address: CS:0108 Operation: INT Dest.: 20 Source:
INT n – Interrupt Type
n=20 or 0010 0000
Binary: 1100 1101 0010 0000
Hex: CD 20
**Instruction**: JMP 110

**Address**: CS: 0114

**Operation**: JMP

**Dest.**: 110

**Source**: 

**Instruction Format**  
short 1110 1011 : 8-bit displacement

**Binary**: 1110 1011 1111 1010

**Hex**: EB FA

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**Instruction**: JGE 11A

**Address**: CS: 112

**Operation**: Jcc

**Dest.**:  

**Source**: 

**Instruction Format**  
Jcc – Jump if Condition is Met

**8-bit displacement**: 0111 tttn : 8-bit displacement

**Binary**: 0111 1101 0000 0110

**Hex**: 7D 06