mode instruction MOV CL,20H, which loads register CL with 20H, not the contents of memory location 20H.

8-, 16-, and 32-Bit Memory Operands. Just as the size of the register operands must match, so too the memory operand sizes must match. In the previous example, because register CL is 8 bits wide, we interpret the memory address 20H as representing the byte at this location. However, when used with the instruction MOV CX,[20H], the address is interpreted as the word beginning at address 20H (because the destination operand, register CX, is a word). Similarly, the instruction MOV ECX,[20H] accesses the doubleword beginning at address 20H. Figure 4.1 diagrams these three instructions. Note that, in all cases, the least significant byte of the data is always stored in the starting memory address. This is called little endian format: The “little” end of the number is stored first.

For some instructions, the size of the memory operand is not clear.

INC [20H]; Byte, word, or doubleword at 20H?

For this instruction, there is no CPU register the size of the memory operand can be inferred from. In this case, the BYTE PTR, WORD PTR, and DWORD PTR operators must be specified.

INC BYTE PTR[20H]; Increment the byte at 20H
INC WORD PTR[20H]; Increment the word at 20H
INC DWORD PTR[20H]; Increment the doubleword at 20H

Register Indirect Addressing Modes. The direct addressing mode has the disadvantage of “locking” the memory address into the instruction. A more flexible scheme is to let a CPU register store the (offset) memory address. This is called the register indirect addressing mode.

MOV SI,20H ;First point register SI at memory location 20H
MOV CL,[SI] ;Move the contents of memory pointed to by register SI into register CL

The brackets are used to indicate that register SI should be interpreted as a memory pointer. Figure 4.2 diagrams this instruction. One caution: When registers are used as memory pointers, the 8086 is restricted to using registers BX, BP, SI, and DI. This restriction does not apply to the 386 and later processors.4

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Figure 4.1 The memory operand size must match the CPU register size. In this example, all three instructions reference memory location 20H, but different data is accessed for each.

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<tr>
<td>20</td>
<td>78</td>
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MOV CL,[20H]; CL = 78
MOV CX,[20H]; CX = 5678
MOV ECX,[20H]; ECX = 12345678

---

4When they are operated in Real Mode, this restriction applies to these processors as well.