WEEK	DATE	LECTURE TOPIC	HOMEWORK	LAB
1	1/23/2018	Intro./Number Systems		
		Logic Intro		
2	1/30/2018	Binary Numbers		Lab0: Lab Intro
		Number Conversions		
3	2/6/2018	Logic Gates, 7400 Series		Lab1:Logic gates
		Truth Tables, Schematics	HW#0 due	
4	2/13/2018	Boolean Algebra, DeMorgan's Theorem		
		Amani and Verilog Introduction, Schematics	HW#1 due	
5	2/20/2018	Minterms & Maxterms		Lab2: Combinational Logic / Verilog
		Karnaugh Map Theory & Examples	HW#2 due	
6	2/27/2018	Binary Addition & Adders, Carry Bit		
		Signed Numbers, Comparators, Sign Bit		
7	3/6/2018	Catchup & MidTerm Review		Lab3:
		MidTerm #1	HW#3 due	
8	3/13/2018	Introduction To Latches & Flip Flops		
		S-R Latches & D & T & JK Flip Flops		Lab4:
9	3/20/2018	Spring Recess		
10	3/27/2018	Registers, Counters		
		Simulation & Timing Diagrams	HW#4 due	
11	4/3/2018	State Machine Analysis		
		Verilog Descriptions of State Machines		Lab5:
12	4/10/2018	State Machine Designs with Mealy & Moore		
		State Machine Designs with Mealy & Moore	HW#5 due	
13	4/17/2018	Catchup & MidTerm Review		Lab6: State Machines
		MidTerm #2		
14	4/24/2018	LEDs & Seven Seg., Resistors, Decoders		
		Buffers/Drivers, Tri-State Devices ALUs and output Flags -NCVZ	HW#6 due	Lab7:Project
15	5/1/2018	Memory & Data Transfers, Basic CPUs		
		Microprocessor Instructions & Opcodes, Registers and I/O Devices		
16	5/8/2018	Project Presentations		Lab Project Presentation
		Project Presentations	HW#7 due	
17	5/15/2018	Final : 10:15am ~12:15pm Tuesday 5/15		
		Final : 8am ~10am Thursday 5/17		

General Notes: Homework from selected sources

References
Mano

OpenSourceBooks
Digi
Digital Logic
Exp
Reference

EEE64-CpE64 Syllabus
EEE64-CpE64 Website

EEE64-CpE64 ECS Webclass