Please Turn Your Mobile devices Silent
CSc/CpE 142
Advanced Computer Organization

Dr. Behnam Arad
Lecture 1

- Introduction
- Course outline
- Computer accounts
- Abstraction/terminology
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- E-mail Address: arad@csus.edu
- Course webpage
  - http://ecs.csus.edu/~arad/csc142

- Office Hours:
  - Posted @ http://ecs.csus.edu/~arad
Text book & Reference


Grading policy

- Projects/Quizzes/Graded Assignments: 25%
- Exam 1: 25%
- Exam 2: 25%
- Final Exam: 25%
Course Description

Design and performance issues of computers. Topics include instruction set architecture, computer arithmetic, processor design, survey of contemporary architectures, interfacing I/O devices, hierarchical memory design and analysis, parallelism and multiprocessing, distributed systems, techniques for enhancing performance, and an introduction to EDA tools for design and verification of computers. Students will design and simulate a microcomputer in an HDL. Cross-listed as CPE 142, and can be taken only once for credit.
Prerequisite

- CSC 137 (for CSc students),
- CPE 166 & CPE 185 (for CpE students), or equivalent.
- Students without proper prerequisite will be dropped from the course.
Course Policies

- Class is attendance required.
- Adjustment to this syllabus or assignments will be announced in class.
- Check your E-mail messages regularly
- Exams will be closed book/closed notes.
- No make-up exam will be arranged unless there is a serious and compelling reason. The instructor must be notified prior to the exam, otherwise no make-up will be given.
No Smart Phone Usage

- Texting
- Surfing the web
- Email
- Etc…
- All Phones must be Silent during the lecture
Laptop Usage

- Laptop usage is allowed only to access lecture slides or to take notes.
Graded Assignments

- Graded assignments should be submitted as one PDF file through SacCT. You can learn about SacCT submission by visiting [http://www.csus.edu/sacct/](http://www.csus.edu/sacct/).

- Each assignment should be typed and have a cover including the following information: Course number, Section, instructor, assignment number, due date, date submitted, and your name.

- Unless otherwise noted, late assignments submitted within one week of the due date will receive a 5% deduction. Late assignments will not be accepted once the solution has been provided.

- For certain assignments, a subset of problems may be graded at random.
Some assignments may require hardcopy submissions as well. This will be explicitly mentioned in the assignment.

Hardcopy deliverables are due in the CSc main office (RVR 3018) by 4 pm on the due date. Time stamp the cover and drop the assignment in the CSC drop box (CPE/EEE students please use CSC drop box as well)
Work Independently

- All assignments and projects must be your independent work. All incidents of academic dishonesty will be dealt with according to the CSUS academic honesty, policy & procedures.

- The minimum sanction for each incident is that no credit will be issued to all students involved for the assignment/project. The university policy is posted at:
  
  http://www.csus.edu/umanual/AcademicHonestyPolicyandProcedures.htm

- Review information provided by the Office of Student Conduct
  
  http://www.csus.edu/student/osc/
Mailing list

- `csc142`
- **Exclusively used by the instructor**
- **To subscription visit**
  
  [http://hera.ecs.csus.edu/mailman/listinfo/csc142](http://hera.ecs.csus.edu/mailman/listinfo/csc142)
You must obtain a Riverside Hall Key Access (FOB) to be able to access the labs.

- Lab 2001
- Lab 3009

You must deliver the approved forms to the Customer Service Center in the Facilities Services Office to pick up the key.
<table>
<thead>
<tr>
<th>Major Topics</th>
<th>hours</th>
<th>References</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction (history &amp; Overview)</td>
<td>1</td>
<td>Chapters 1 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Instruction Set Architecture</td>
<td>1</td>
<td>Chapter 2 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Performance evaluation</td>
<td>3</td>
<td>Chapter 1 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to Computer Arithmetic</td>
<td>4</td>
<td>Chapter 3 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to Modeling in Verilog</td>
<td>4</td>
<td>Verilog HDL by Samir Palnitkar</td>
</tr>
<tr>
<td>CPU Design (Datapath &amp; control)</td>
<td>10</td>
<td>Chapters 4, and Appendix D Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Memory Design and Analysis: <em>Cache, virtual, and Interleaved memory</em></td>
<td>9</td>
<td>Chapter 5 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Interfacing and Communication</td>
<td>5</td>
<td>Multiple chapters and Lecture slides from the 4th edition Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Parallelism</td>
<td>3</td>
<td>Chapter 6 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Introduction to distributed systems</td>
<td>3</td>
<td>Chapter 6 Patterson &amp; Hennessy</td>
</tr>
<tr>
<td>Survey of contemporary architectures</td>
<td>2</td>
<td>Multiple Chapters Patterson &amp; Hennessy</td>
</tr>
</tbody>
</table>
Von Neumann architecture

Von Neumann Architecture reference:
http://en.wikipedia.org/wiki/Von_Neumann_architecture